Zachodniopomorski Uniwersytet Technologiczny w Szczecinie

WYDZIAŁ INFORMATYKI

Faculty Of
Computer Science
And Informationtechnology

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PhD Thesis

Rozprawa doktorska

Hybrid Optimization Algorithms applied to Model Reduction of EMI in GALS Systems

Wykorzystanie algorytmów optymalizacji hybrydowej do modelowania redukcji zjawisk interferencji elektromagnetycznej w układach GALS

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Szczecin, 2014

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Abstract

This dissertation investigates and presents the possibilities of reducing EMI in GALS systems and its further automation by using a hybrid optimization. Several different abstract models of GALS circuits have been designed in order to extract a realistic pausable clock behavior. An advanced tool for analyzing EMI GalsEmilator has been created in order to investigate the current profile of each modeled system according to clock behavior. The research has been conducted both in frequency and time domain. As a result, a reduction up to 26 dB can be achieved when applying a low-EMI GALS methodology and the process of selecting GALS systems parameters can be automated in order to achieve the best results.

Key words: GALS, EMI, current peaks, asynchronous design, hybrid optimization

DECLARATION

I hereby declare that I wrote the submitted PhD Thesis independently. During my work I have not, apart from necessary consultations, used any help from others; I have not instructed anyone to write or correct any of the following chapters. I have not copied any parts of the PhD Thesis from other authors. I also confirm that both paper and electronic copies of the submitted manuscript are identical. I understand that making a false declaration in this case will result in revocation of the decision to issue the diploma.

OŚWIADCZENIE

Oświadczam niniejszym, że przedkładaną pracę doktorską napisałem samodzielnie. Oznacza to, że przy pisaniu pracy poza niezbędnymi konsultacjami, nie korzystałem z pomocy innych osób, a w szczególności nie zlecałem opracowania rozprawy lub jej części innym osobom, ani nie odpisywałem rozprawy lub jej części od innych osób. Potwierdzam też zgodność wersji papierowej i elektronicznej złożonej pracy. Mam świadomość, że poświadczenie nieprawdy będzie w tym przypadku skutkowało cofnięciem decyzji o wydaniu dyplomu.

Contents

1. Introduction

From the time when the first silicon chip was invented, there has been a continuous improvement and miniaturization of that technology. In recent years the manufacturing process has become more and more advanced leading to miniaturization of the systems which proves challenging for the system designers. The basic synchronous approach in chip design became more challenging because of problems with its dimensions. It turned out that the most problematic is the size of a clock tree and fulfilling proper timing constraints. Moreover, because of the miniaturization the chips are more prone to a noise generated by digital components. Hence, a new methodology had to be applied to decrease the level of EMI (Electromagnetic Interference). The GALS (**G**lobally **A**synchronous **L**ocally **S**ynchronous) approach has been presented as a solution for the system design many years ago [7], [49]. It has also been proposed to utilize GALS systems for EMI (**E**lectro-**M**agnetic **I**nterference) lowering in digital circuits [1]. Several examples have shown that asynchronous design can significantly reduce EMI in comparison to the classic synchronous design, one being - an asynchronous design of an ARM9 processor - Amulet 2 [2]. Some initial studies regarding the GALS approach for EMI reduction have been conducted [1]. Those have shown that the GALS systems can achieve EMI reduction of up to 20 dB in comparison with a synchronous design. In time domain, the noise peaks can be lowered up to 40%. Initial studies and real on-chip measurements [3], [4] have shown about 5 dB smaller reduction of EMI. However, further investigation proved the possibility of EMI reduction at the level of 26 dB [26], [3].

Moreover, those activities were not systematic and were focusing only on specific design cases, not taking into consideration GALS as a general methodology for system integration. The technology advance and further device miniaturization increases a demand for deep investigation of EMI because of its detrimental influence on a whole system performance.

Initial studies have been completed to use FPGA (Field Programmable Gate Area) technology as a testing platform for GALS systems [28], [29]. However, it transpired that FPGA has a lot of drawbacks regarding GALS implementation [29], mainly because of poor clocking systems in FPGA chips [30] and complicated routing schema. Thus fur-

ther exploration of FPGA as a testing platform has been dropped and focus is now on ASIC technology.

Moreover, there are no dedicated tools to model EMI in GALS and synchronous circuits on a high abstraction level. It is needed to have the possibility to predict at least approximate values of EMI in designed digital systems. In synchronous systems, which are much more evaluated because of their wide application, it is easier to estimate EMI. There are many investigations showing the possibility of reduction of EMI in synchronous systems by adding clock skew and phase modulation of the clock [33], [6]. However, adding a clock skew or a phase modulation of a clock to a synchronous chip demands additional work and sometimes generates very difficult problems in timing closure.

1.1. Theses and dissertation's objectives

The theses of this work were formulated as follows:

> In this dissertation it is assumed that it is possible to set such parameters of GALS digital systems that the EMI generated by these systems is evidently lower than in synchronous digital systems without applied features to reduce EMI. Moreover, the process of selecting parameters of GALS system can be automated by using hybrid optimization algorithm. The final result should be a set of reasonable parameters of GALS system that generate EMI evidently lower comparing to its initial state.

In order to prove such a thesis partial aims are defined as follows:

- *present GALS system architectures impact examination for possible EMI reduction*,
- *proposition of an optimizing hybrid method used to reasonable selection of GALS system power control parameters to reduce EMI at the stage of digital system design*.

It means, that the aim of this work is facilitating cross-benchmarking of EMI features for GALS and synchronous design style. It is important to make such EMI analysis,

which would let system designers choose solutions optimal for their needs. The first step to prepare this is to create software able to model and evaluate EMI in synchronous and GALS systems. In my dissertation, I would like to present a software tool able to simulate the EMI behavior caused by clock activity in GALS and synchronous systems on a very high abstract level. This tool is able to model additional features such as introduced jitter, pausable clock, phase shift that can be embedded into GALS or synchronous systems in order to reduce EMI characteristic.

This tool enables performing many simulations in order to investigate the best way to reduce EMI in GALS and synchronous circuits. Several GALS topologies have been evaluated and compared to their synchronous counterparts.

However, performing manually thousands of simulations is not an efficient way to obtain fair results. Thus, a hybrid optimization algorithm has been proposed to automate the process in order to facilitate circuit designers' decisions. It allows setting ranges of parameters e.g. frequencies of each GALS block and running hundreds of simulations in order to obtain the best results regarding EMI reduction in GALS systems. Such a technology moves us a step forward in the design of electronic GALS circuits in the matter of reducing EMI.

The dissertation is structured in a following way: Chapter 2 describes GALS methodology, its structure, components and behavior. Additionally, EMI in digital circuits, its sources and the possibilities of its reduction are presented. This chapter also includes a case study. In Chapter 3, the accurate (not only mathematical) models of GALS systems are discussed, and the software used to model EMI is presented. Moreover, a hybrid optimization algorithm, applied in further investigations, is described. In Chapter 4, the results of simulations for different GALS topologies, different granularities of digital systems, various EMI reduction methods applied, are presented and compared with synchronous designs. Furthermore, results of hybrid optimization algorithm are shown. In final section conclusions are drawn from the data presented throughout the paper.

2. GALS Systems and EMI sense

In this chapter the issues of GALS systems and EMI in digital circuits are explained [20]. First, the GALS methodology is described. The instances of GALS interfaces are demonstrated. In particular, port controllers and local clock generators are presented. In addition, modeling of current shapes is explained regarding EMI in digital circuits. The possibilities and methods of EMI reduction in digital circuits are described: especially, clock generator modifications are pointed out. For instance, clock skew and phase modulation applicable to digital circuits are presented. In the chapters' conclusion a case study is demonstrated.

2.1. Introduction to current GALS methodology

GALS is quite an original technology for VLSI class circuits designing, it is not well defined yet [35], [63]. GALS systems are a compromise linking totally synchronous design and the asynchronous one [39], [50]. Therefore GALS builds on the advantages of both systems [52]:

- *GALS are easy to integrate*, because of an asynchronous communication any existing synchronous chip can be utilized and combined with any other without concerning the frequency at which they are supposed to work.
- *GALS are useful for existing synchronous solutions regarding its structure*; it is possible to use any synchronous design and with only minor changes adopt it to work as a Locally Synchronous (LS) island in GALS systems [44].

However, GALS is not only a class of circuits, but also a methodology that is still not well defined and investigated [62] e.g. in the field of EMI and subsequently it is not widely used. The potential is known but the lack of predefined libraries and standards does not encourage commercial companies to use it as a possible solution for market products.

It is generally stated, that GALS consists of combining multiple synchronous blocks through an asynchronous communication [38], [47], [54]. It does not define any

specific way in which the communication should be driven by two adjacent blocks. For that reason several solutions, presented in subject literature, can be found:

- S. Smith [13] presents a GALS system without pausable clocks. Instead, synchronizers are used to avoid metastability. Also Chattopadhyay [14] describes similar design where bidirectional asynchronous FIFO [48], [61] components are used to avoid metastability.
- A specific approach has been presented for data path architectures. A communication circuit presented by M. Krštić [3] is able to process big data frames as a batch. After a burst data transfer a period of inactivity occurs. The local clock is obtained through a specific handshake. Therefore, there is no necessity to use any additional clock generator. A similar approach has been also proposed by J. Kessels [15].
- S. Moore et al. [16] proposed GALS system utilizing a 2-phase bundled data communication approach. A ring oscillator [60] acting as a pausable clock generator was used to prevent metastability during data synchronization between two adjacent modules. Another version of that approach has been presented in [42].
- D. Bormann [17] presents a GALS system utilizing as a 4-phase bundled asynchronous data communication. Pausable local clock generators [34] are used in order to prevent metastability during a handshake between adjacent blocks [45], [47], [46]. J. Muttersbach [7] describes a similar approach in his thesis. He defines precisely the structure of GALS systems with different port types.

For the purpose of this PhD Thesis, methodology described by J. Muttersbach [7] will be used when discussing GALS.

In Figure 2.1 a basic block of a GALS system is illustrated. At the center of each block a *Locally Synchronous* (LS) Island is placed. It is designed by standard tools dedicated for typical synchronous systems. The LS Island contains the functionality of the whole block. Additionally, the Island is surrounded by a GALS wrapper. The wrapper contains input and output ports controllers, data paths and local clock generators. The local clock generator delivers a clock signal for an LS Island.

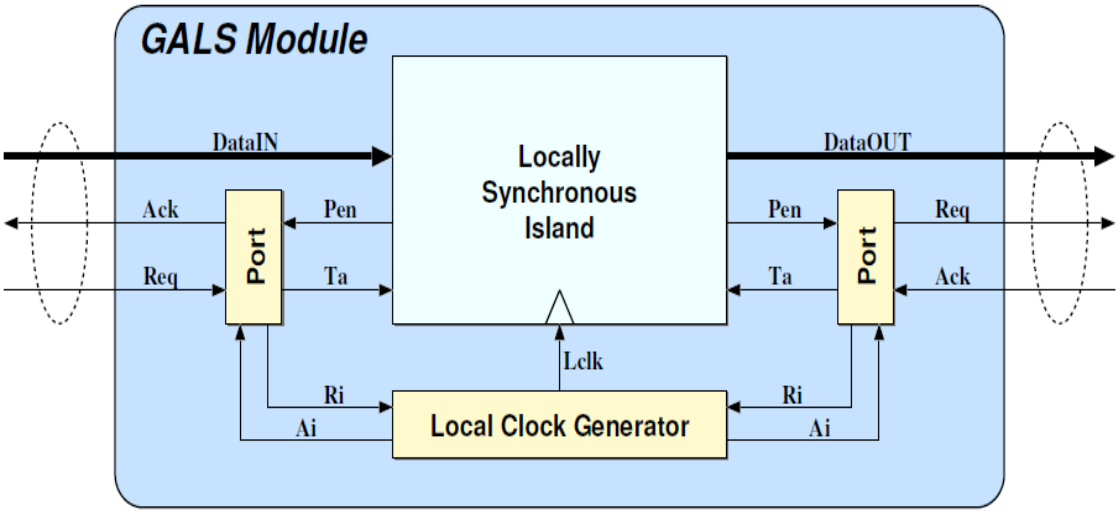

Figure 2.1. An overview of a single GALS module with an input and an output port [18]

Port controllers are used to drive a handshake between adjacent blocks before the data transfer occurs. They are the asynchronous finite state machines (AFSM). In order to prevent metastability and provide a successful handshake, port controllers can stop a local clock generator.

Figure 2.2 presents a timing plot with three successive clock cycles of a D-type output port controller. The port controller is described in details in the next subchapter. In the chart, the GALS block utilizes a four-phase bundled handshake protocol in order to transfer data to a similar GALS block. The most important signals that drive the whole procedure are illustrated and divided into three groups:

- LS Island signals: *Pen* (Port Enable), *Ta* (Transfer Acknowledge from port controller)
- Local Clock signals: *Ri* (Request to a local clock), *Ai* (Acknowledge from a local clock)
- GALS module signals: *Req* (Request to an adjacent GALS module), *Ack* (Acknowledge from an adjacent GALS module)

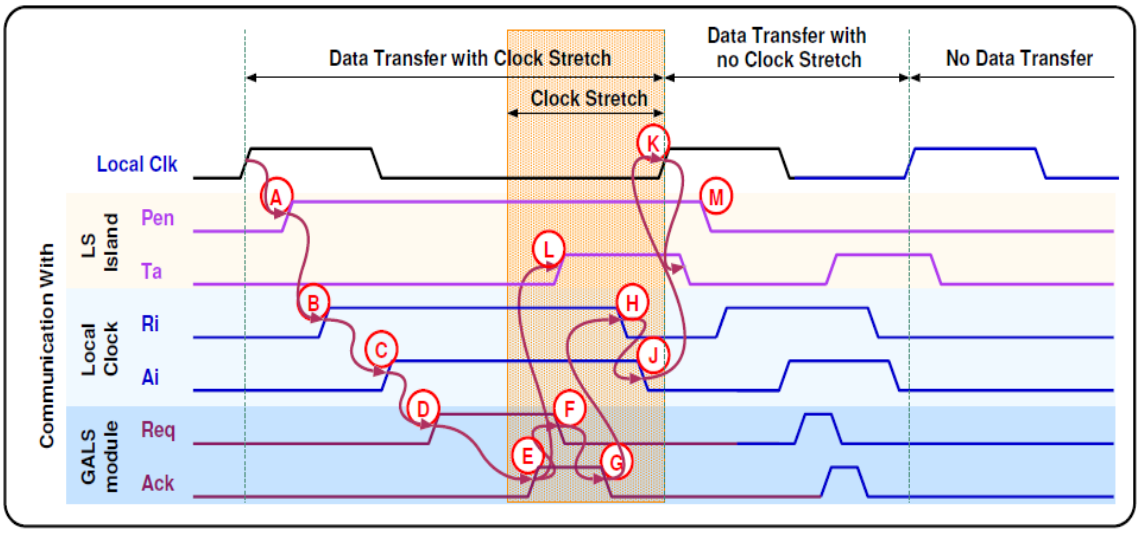

Figure 2.2. Timing for a D-type output controller for three consecutive clock cycles; *In the first cycle shown, the environment is slow to react to the Req signal. As a result the clock is stretched until the data transfer has been processed. The second cycle shows another transfer where the handshake finishes within the clock cycle. Finally in the third cycle, the Pen signal is not enabled, and no data transfer is initiated* [**18**]

Moreover, in Figure 2.2 a Local Clock (*Clk*) signal is presented. Port Enable is utilized by the LS Island in order to trigger the port controller (A). Next, the port controller instantly sends a request signal (*Ri*) to stop the local clock generator (B). When occurrence of a new active edge of the clock signal is prevented, the local clock generator changes a state of the acknowledge signal (*Ai*) to a high-state (logic-1). From that point, no new rising edge of a clock will be generated. The activity of an LS island is stopped. Subsequently, the *Req* signal is activated (D) by the port controller. It informs the receiving GALS module that a new part of data is ready to be transferred. When the receiving GALS module is prepared to accept data, its port controller undertakes the similar steps. It raises the *Ack* signal to the high-state in order to confirm receiving of the *Req* signal from the transferring GALS module (E). As soon as both the GALS modules are paused, the receiving one can safely accept the data. When the transfer is established, the handshakes signals go back to their initial states. The local clocks generators are released and a new clock signals can occur. *Req* is deactivated first at the transmitting side (F). When *Ack* signal is deactivated by next module, the local clock generator

is activated by releasing the *Ri* signal (H). Next, the local clock generator sets *Ai* signal to low-state and starts to generate clock pulses (K). Finally, the port controller informs the LS island about a successfully completed data transfer by setting a transfer acknowledge (*Ta)* signal (L) to a high-state [18].

During the handshake procedure presented above, it can be noticed that the LS Island initiate a data transfer by changing the state of the *Pen* signal. In the first cycle, the handshake is triggered by a rising edge of the *Pen* signal. In the second one, communication is triggered by a falling edge of the *Pen* signal. In the third cycle, no change of the *Pen* signal occurs. Thus, the handshake procedure in that system is triggered by transition of the *Pen* signal. Falling or raising edge of a signal do not affect the outcome. Hence, the data transfer in two phase protocol is doubled in comparison to a standard four phase protocol. This feature is applied only to the *Pen* signal.

During the first cycle in Figure 2.2 the stretched clock can be observed. This situation is caused by the sending block that awaits the Ack signal from the receiving one. It slows down slightly the LS block functionality. However, it ensures that an adjacent block is ready to receive data. That pause of the clock will be analyzed later because it adds a natural phase shift to the GALS system. Pausable clock in several GALS blocks can generate a total disharmony. Even if the frequency of each GALS block would be the same, the pausable clock is able to mix their phases. Hence, pausable clocking can influence EMI in GALS systems.

2.1.1. Port Controller Types

In Figure 2.2 the clock generator is stopped directly after the LS Island is ready for data transferring. This situation is necessary in a system, which cannot continue to operate normally without finishing the current data transfer. According to Muttersbach [7], [8] there are two types of port controllers:

1) '*Demand Type*' (D-type) ports – stop the clock generator directly after they are requested to introduce handshake procedure. These are presented in Figure 2.2 and described above.
2) '*Poll Type*' (P-type) ports – in contrast to the D-type controllers, P-type controller does not stop local clock generator as soon as the *Pen* signal changes its state. It allows the LS island to continue its normal work until a data dependen-

cy appears. First, when the *Pen* signal transition occurs, the port controller sends a request to an adjacent block. It does not stop a local clock generator until the acknowledge signal (*Ack*) comes from an adjacent block. When a rising edge of the *Ack* signal occurs, port controller immediately generates a high state of the *Ri* signal in order to stop a local clock generator. Then a typical four-phase handshake follows. When the data transfer is established, all signal values return to their initial states.

2.1.2. Local Clock Generator

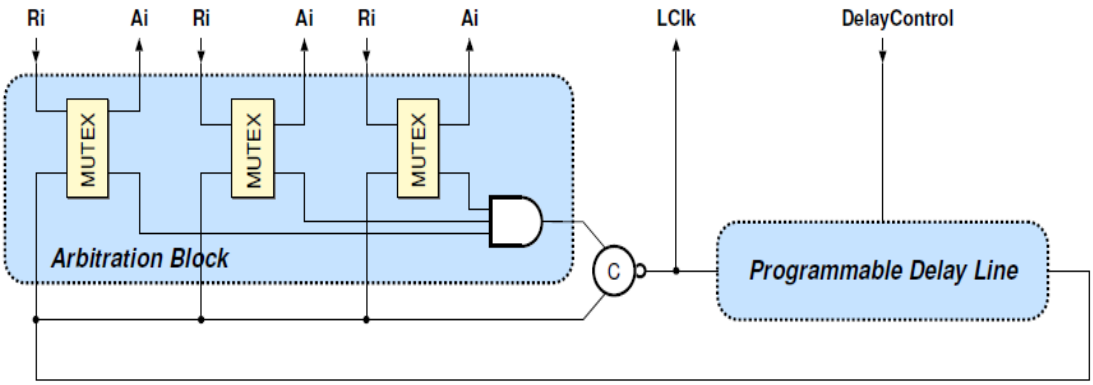

Figure 2.3. Simplified block diagram of a pausable local clock generator [18]

In order to prevent metastability in GALS systems during data transfer, Pausable Local Clock Generator has been introduced to the system by Muttersbach [7]. Hence, port controller can easily operate having an ability to stop the LS island when it is necessary and successfully complete the data transfer between the adjacent GALS blocks. In Figure 2.3, created by Gurkanyak [18], a simplified block diagram of a pausable local clock generator is presented. It is generally a ring oscillator with a Programmable Delay Line. The Delay Line is used to set the period of the clock. An Arbitration Block allows each port controller to pause a clock in order to conduct a handshake protocol without introducing metastability to a system.

The usage of a ring oscillator as a Local Clock Generator is a very rational approach to EMI reduction. It allows each GALS block to work with its own frequency and phase [36]. Thus, the frequency spectrum of a whole chip is spread and lowered.

The Local Clock Generator contains several input and output ports accordingly to the number of port controllers in a GALS wrapper. Each of the port controllers has

the ability to pause the clock generator by applying the high-state to the request signal (*Ri*). The signals connected to the port controller are joined with an output of Programmable Delay Line through a **Mut**ual **Ex**clusion Component (MutEx). MutEx is a specific element that propagates only one high state signal during a fixed time. For that reason, when a request to pause the clock has been introduced, no positive clock edge would appear. Several implementations of the MutEx have been presented in the literature i.e. [18]; those will not be discussed in detail as they fall outside the scope of this thesis.

There is only one possible state of all the *Ri* signals when the local clock can be propagated through the arbitration block. The *Ri* signals must be in the low-state in order to avoid blocking of a rising clock edge by *MutEx* element. The Arbitration Block is further connected with a Muller-C component that changes its state only in case when both the signals have the same state. The local clock generator will be paused as long as one of the *Ri* signals remains in high state (logic-1). The MutEx informs the port controller if the pausing of local clock generator was successful achieved by changing acknowledge signal (*Ai*) to high-state (logic-1). As long as *Ai* is at high-state the clock will be paused. When the port controller lowers *Ri,* after a while *Ai* is also lowered and a new rising edge of the clock generator can occur.

The local clock generator is mainly interesting because of its ability to set defined frequency of a clock by adjusting a programmable delay in line. This in turn facilitates programming different GALS system by changing only one value per GALS module. In several GALS topologies that are described later, this advantage of GALS system has been employed. It speeded up modeling of GALS systems with different sets of frequencies.

Although, the maximum number of ports of a pausable clock generator is not defined, connecting the outputs from too many ports controllers decreases the highest achievable clock frequency. In practice, local clock generators with up to 8 ports have been designed and investigated [18].

Recently a new approach for Pausable Local Clock Generator has been proposed by E. Grass et al. [1]. Instead of an internal local clock generator (presented before), a new externally clocked wrapper has been proposed. It delivers a clock to different GALS blocks with the same frequency but with a different phase. However, it is not a desired

solution for GALS systems where the most important issue is an EMI reduction. The main drawback of this solution is the same frequency for the whole digital circuit.

2.2. EMI in digital circuits

An EMI phenomenon in digital systems is caused generally by the simultaneous switching of logic components [33]. Each active edge of a clock pulse, in a synchronous system, triggers all flip-flops that generate noise. This triggering is not exactly at the same moment because of the clock tree and its skew that spreads triggering of the flip-flops in time [55]. The easiest way to analyze EMI generated by the digital circuits is to evaluate the sources' current shape. Reduction of EMI is possible in several ways including improvement of physical elements. However, I have focused in my thesis only on the modification of a clock behavior by adding a jitter or a fixed phase to each sub block.

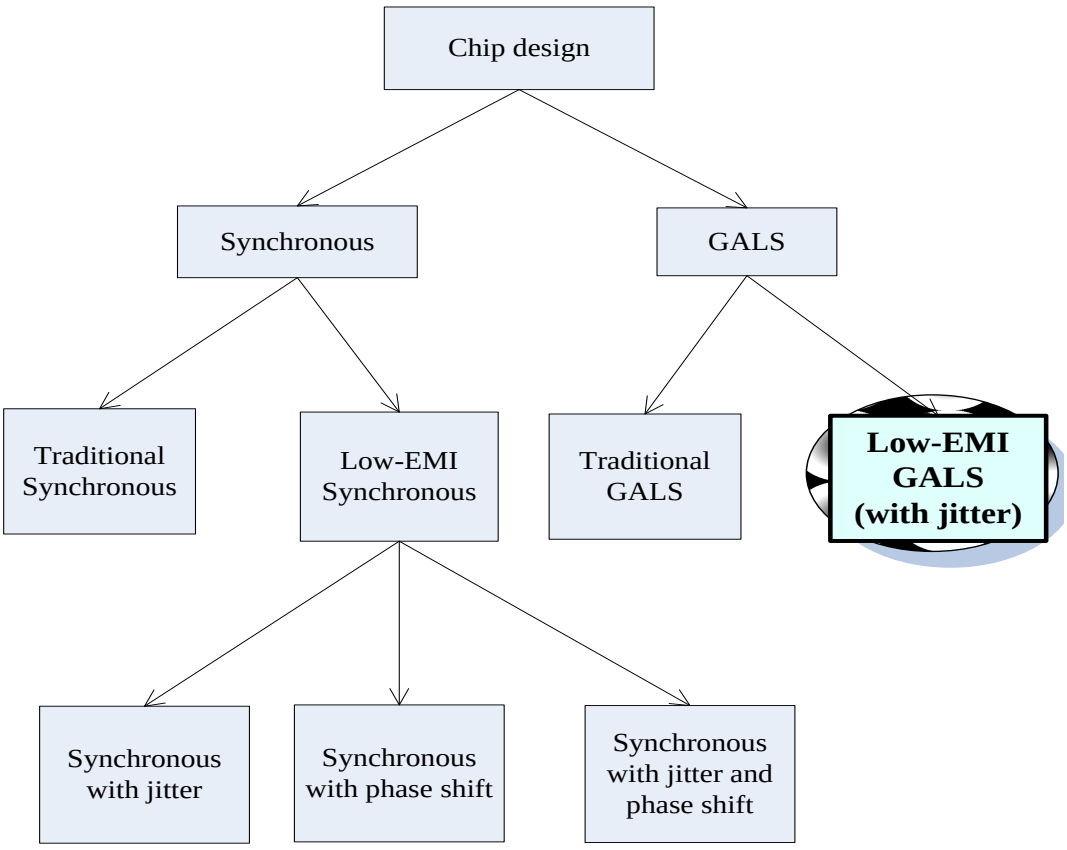

Figure 2.4. Chip design styles concerning EMI reduction, where Low-EMI GALS systems are the object of this dissertation

In Figure 2.4 various chip design techniques concerning EMI reduction have been presented. First circuits can be divided into GALS and Synchronous systems. GALS systems are understood as a number of sub blocks that can operate with different frequencies and with pausable clocks. Thus, applying a phase shift to a GALS sub block would have no impact on EMI reduction. Phase shifting is in nature of GALS systems. For that reason, GALS chips are divided into the traditional ones and Low-EMI GALS with jitter applied. On the other hand, the synchronous systems can be divided into the traditional ones and Low-EMI. A traditional synchronous system represents a circuit with one clock domain. The clock tree is usually so spacious that a natural clock skew occurs. Low-EMI synchronous systems are further divided into three categories according to incorporated features. Therefore, a synchronous system can contain:

- Jitter
- Phase shift
- Jitter + phase shift

2.2.1. Modeling of current shape

In order to construct a more realistic model of EMI of any digital system, an accurate current shape profile is required. The current shape profile describes the power consumption of a circuit in a time domain according to its activity during a clock cycle [32], [52]. Having the power consumption of a system in a time-domain [5] it is possible to estimate EMI, which is directly caused by the activity of the circuit.

$$\frac{tr}{tf} = \frac{Nr}{Nf}, \qquad N_r, N_f \in N$$

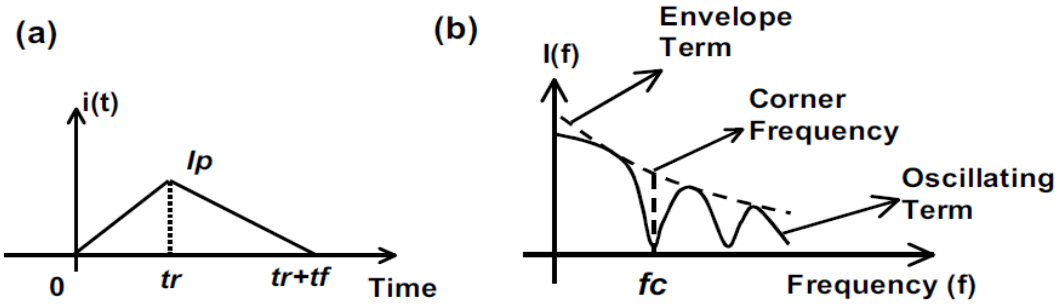

Figure 2.5. Triangular approximation of the supply current in (a) time-domain and (b) frequency domain [10]

However, it is very difficult to define the current shape for each digital block and in each clock cycle, when the system is defined on a very abstract HDL level. The current profile varies significantly in each design. Additionally, it can change from cycle to cycle depending on activity and processing load [41]. For that reason, one of the most challenging tasks is to model a current profile in each clock cycle. In [33], [10] it is presented that for digital circuits triangular modeling of the current shape can be sufficient. In Figure 2.5 triangular supply current is presented both in time-domain and frequency-domain. The *Ip* point is a current peak, *tr* is a increase time, *tf* is a decrease time. It is said that generally *tr* takes 25% of processor cycle, *tf* takes 50% of processor cycle and 25% is necessary for stabilization of all signals and responsible for that action flip-flops. This scheme is presented in Figure 2.6.

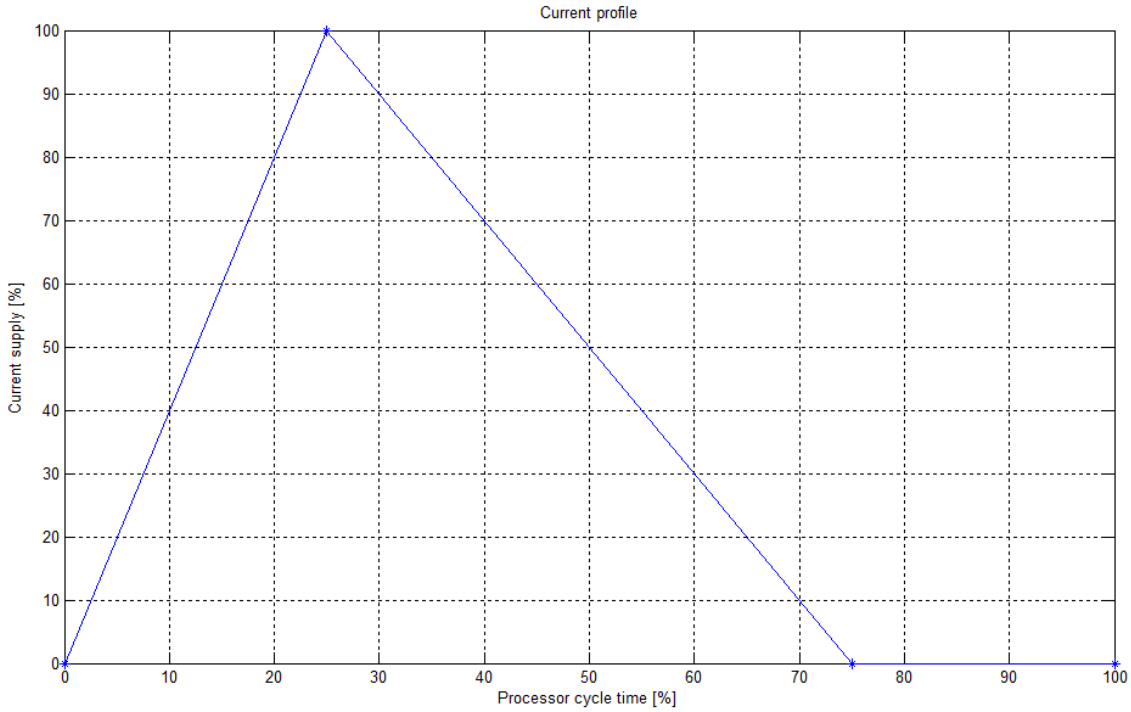

Figure 2.6. Sample model of a current profile of a processor cycle

Moreover, in Figure 2.7 frequency spectrum of different current waveforms is presented. It can be observed that a reduction of amplitude in frequency domain can be achieved by applying different shapes of waveforms. The lowest values are presented with square waveform, whereas the highest with triangular and pseudo random waveforms. Thus, the more flat current shape, the lower values in the frequency domain.

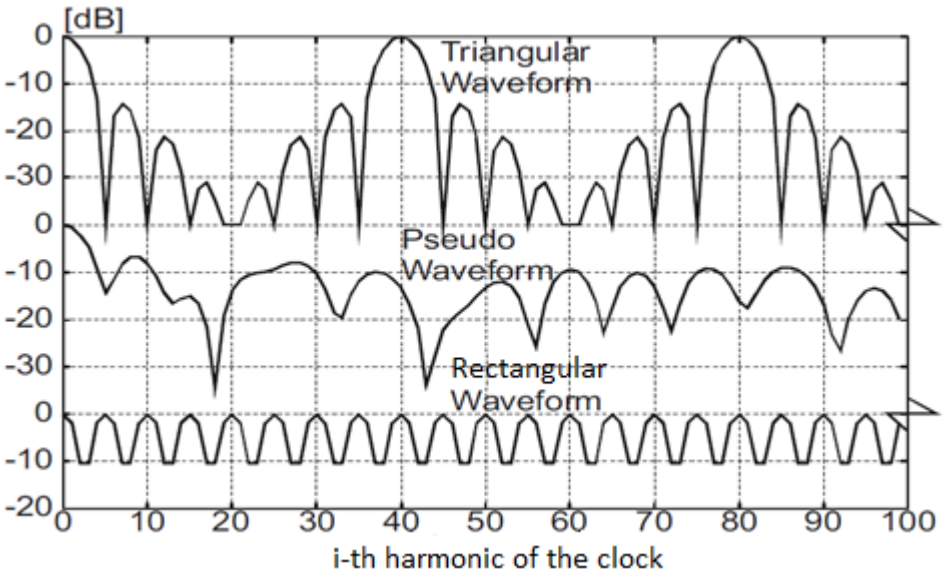

Figure 2.7. Frequency spectrum of the different modulating waveforms: Triangular, Pseudo Random and Rectangular [10]

However, the results presented above are too general. Depending on the logic activity in the chip there can be totally different current shapes for each clock cycle. For instance, the triangular model cannot always emulate real behavior of the digital circuit. The current profile could be modeled as a superposition of two or more triangular shapes for some elaborated systems [11].

To support this assumption a realistic digital synchronous circuit has been modeled. It was composed of:

- Complex sequential stage (512 flip-flops)
- Combinational logic (813 basic combinational cells)
- Reset
- Clock tree (369 buffers)

The circuit has been modeled by Miloš Krstić in 0,25 μm CMOS technology from IHP (Institute for High Performance, Frankfurt (O), Germany) and simulation was completed in different scenarios in Cadence Spectre [11]. Two examples are shown in Figure 2.8. The current shape from 1a) can be modeled as a triangular shape, however, for 1b) a more precise model would be the superposition of two triangles.

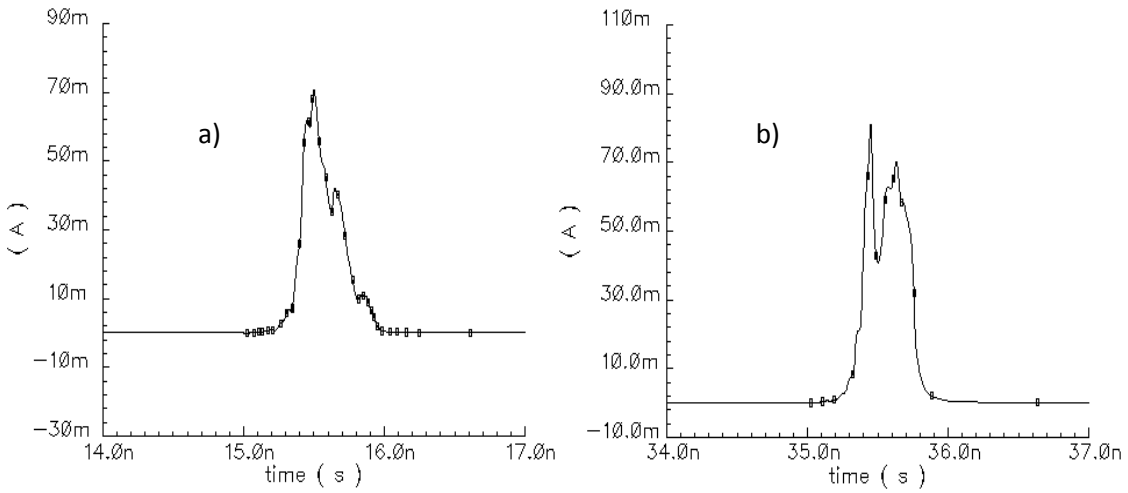

Figure 2.8. Analog current profile simulation using 0.25 um CMOS process [11]

2.3. EMI reduction methods in digital circuits

Generally, there are two categories of methods that are able to reduce EMI in digital circuits (Figure 2.9) [10]. First one is classified as passive methods, based on adding a special material to a digital circuit (usually on PCB) in order to diminish EMI effect. Passive methods impact only the effects of EMI occurrence. The second category is known as active methods which impact causes of EMI.

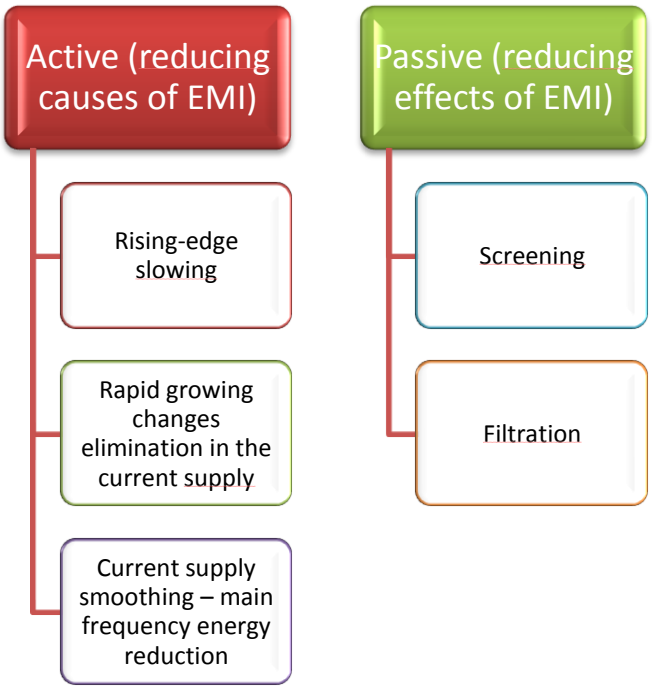

Figure 2.9. General methods of reducing EMI in digital circuits

2.3.1. Passive EMI reduction methods

There are two main passive methods: screening and filtration [51]. Screening is a mechanical solution, depending on adding special fabrics to a digital circuit in order to prevent spreading of EMI among different parts of digital circuit e.g. paths, input/output signals, signals with different characteristics, parts of PCB or even blocks of processors. Filtration on the other hand, depends on filtering unwilling range of frequencies that can occur because of electromagnetic interference in a circuit. Set of rules for digital circuit designers regarding passive methods application can be found in literature [21]:

- connect unused recurring operational amplifiers inputs to ground, and connect the inverted inputs with outputs,
- filter signals from noisy sources,
- filter all signals connected to PCB/processor,
- place buffers and I/O controllers directly by the I/ O connectors on the edges of the PCB,
- place clock generator in the middle of the PCB,
- separate the sub-systems according to their operating frequencies and level of signals,
- provide separation/screening between signals with high noise and low noise,
- provide separation/screening between digital and analog signals and place them away from each other,
- place clock signals paths and digital signals paths away from analog inputs and reference voltage inputs,
- place clocking systems away from the I/O connections,
- minimize the length of critical paths (blocking capacitors should be placed as close as possible to the IC),

- use all power terminals,
- use a twisted-pair cable to minimize feedback, if it is possible,
- use additional ground connections to reduce the coupling between signals in connectors,
- use short and simple lines with RF signals,
- avoid placing paths under quartz generators,
- avoid carrying sensitive signals in parallel to the fast-changing signals,
- use wide paths for critical signals and provide parallel ground paths on both sides.

2.3.2. Active EMI reduction methods

Active methods are used to prevent occurring or to reduce the occurrence of EMI in digital circuit. They impact the causes of EMI. First of all, the EMI can be reduced as a result of a slowing signals' rising edge. The power of main harmonics is dissipated in a wider frequency range. However, it is a risky method where glitches can appear (can generate additional transients) and signal/system noise to power ratio is reduced. Thus, that method is not recommended in most practical digital solutions.

The most popular method is eliminating rapid changes in current supply. It can be archived, for instance, by spread clocking (*forced spread over time of rising edge supplying individual components in digital electronic circuit*) [58].This method consists of spreading the clocking signal into a wider range of time among the processor. It is a common technology used in most computers nowadays because it doesn't require any additional processor components to achieve good results. It requires only special design of an integrated circuit where clocking signal paths are placed according to the delay they generate. Thus the **S**imultaneous **S**witching **N**oises (SSN) [57] are spread over time between different parts of the processor. However, this technique also requires designers to take care of timing constrains which are the most significant to keep the proper working of flip-flops, its set-up time, of whole integrated circuit. This technique is applicable mainly in synchronous designs with one clock domain.

Finally, current supply smoothing methods can be utilized to reduce EMI in digital circuits. It is similar to rapid current supply changes elimination but puts more effort on smoothing the whole current supply wave. First of all, a **S**pread **S**pectrum **C**locking (SSC) [56] can be utilized. It depends on spreading the clocking signal into a wider range of frequencies and it is called jitter. SSC depends on changing the clocking frequency according to a special pattern. It can be either a pseudo-randomized selecting solution or a deterministic one, for instance triangular selection, where a modulating signal has a triangular shape. This technique can be used both in synchronous or asynchronous designs. The next method of smoothing supply current signal is applicable only in asynchronous designs, such as GALS systems, where different sub-blocks work with different frequencies and continuous phase shift of clock signals among sub-blocks.

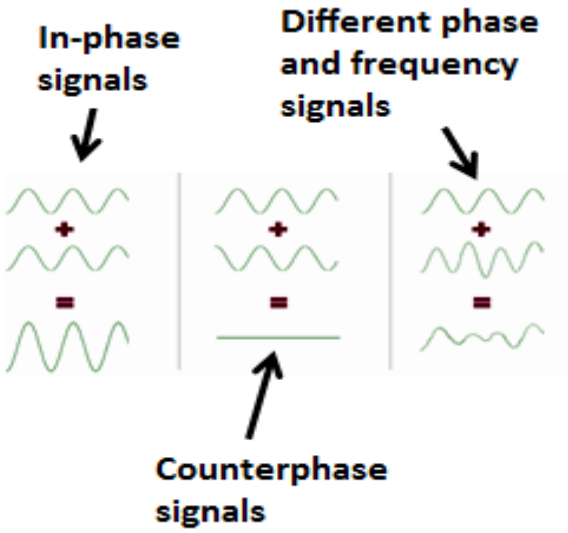

Figure 2.10. Sample mutual influences of two electric signals

As it is presented in Figure 2.10, when two similar signals are in-phase then their amplitudes are added and create signal with a double power. It can be assumed that a synchronous processor is combined with a number of such in-phase signals, thus generates strong current peaks and high EMI. On the other hand, there are two out-of-phase signals which generate a constant waveform with only one peak in a frequency domain. It is an ideal solution with constant current supply requirements. However, achieving such a waveform is almost impossible in real life where processor contains

thousands of flip-flops. But it is possible to get close to those results by shifting a clock signal in phase among different parts of processor. Traditional synchronous design could not stand such a solution because of restrictions in timing-constraints. GALS technology is able to do that and also provide a possibility to apply different frequencies to each sub-bloc. This solution deepens a smoothing of current supply waveform.

2.3.3. Applied techniques

It is said that two main techniques are used to reduce EMI in synchronous systems by modifying clock behavior [1]. First a clock phase shift can be added to each LS block. Phase shift decreases the current peaks for a whole circuit, thus reducing EMI. Additionally, jitter can be added to the clock source [10], [19].

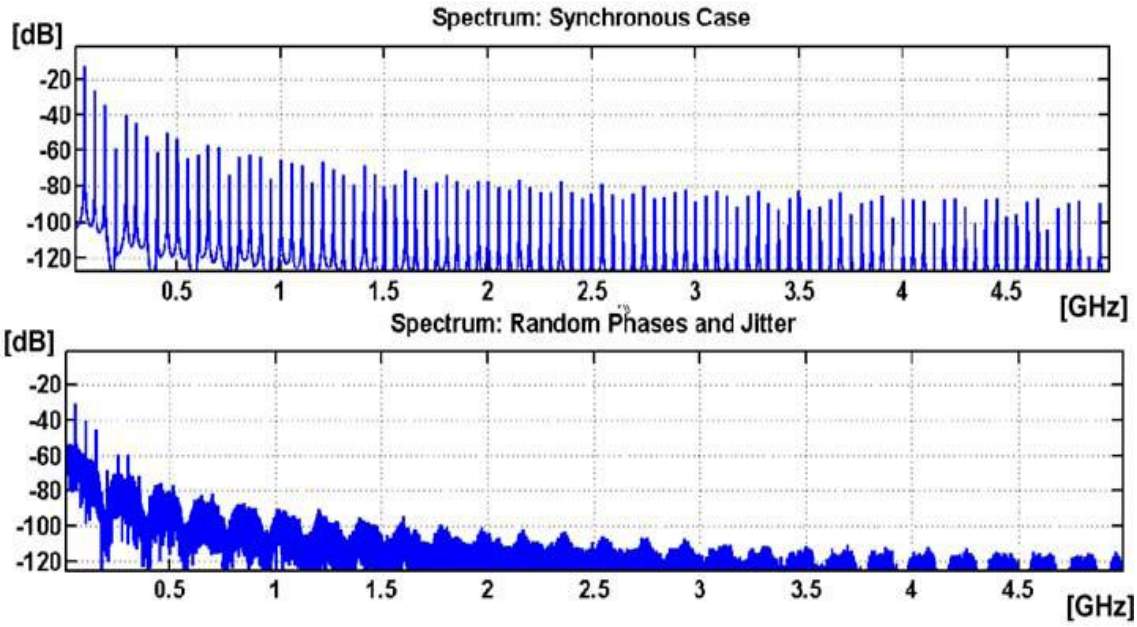

Figure 2.11. Power spectrum of supply current for synchronous circuit (top) and its equivalent GALS implementation (bottom) [1]

The results of combining both of those features in a GALS system in comparison with a synchronous approach has been presented in Figure 2.11 [1]. It is clear that EMI can be reduced up to 15 dB. However, the GALS system utilized in that model was firmly simplified with respect to the full potential of GALS systems. It was assumed that all 10 sub blocks operate with the same frequency (50 MHz). Thus, it resembles more a synchronous approach than a GALS system. The possibility of different clock generators (different frequencies) for each sub block regarding EMI reduction was also not investi-

gated. Moreover, applying a phase shift to each sub block indicates that GALS pausable clock was not analyzed too. Therefore, it is safe to conclude that more detailed investigation is required to fully analyze the possibility of EMI reduction in GALS systems.

2.3.4. Jitter generator

Jitter (Figure 2.12) introduces a phase modulation (most often random rapid phase fluctuations) to a clock wave from cycle to cycle (Figure 2.13). It influences EMR (Electromagnetic Radiation) [10]. Jitter modifies slightly, up to a defined part of a period, the starting point of a rising edge, while the time of the high level stays constant [31], [59]. Hence, jitter can increase or decrease the clock period for a cycle but the average base frequency remains the same. The change can be generated either randomly or deterministically.

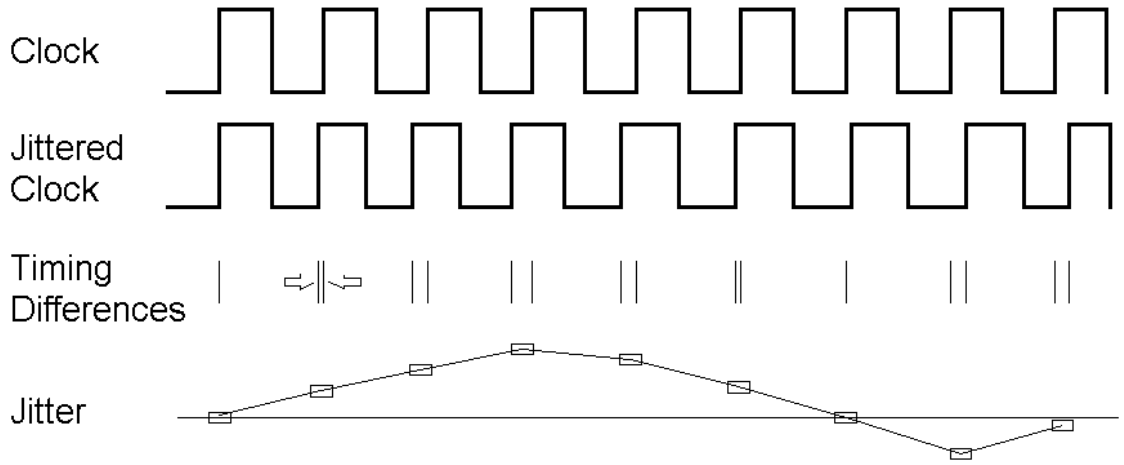

Figure 2.12. Jitter; phase variations between two signals [24]

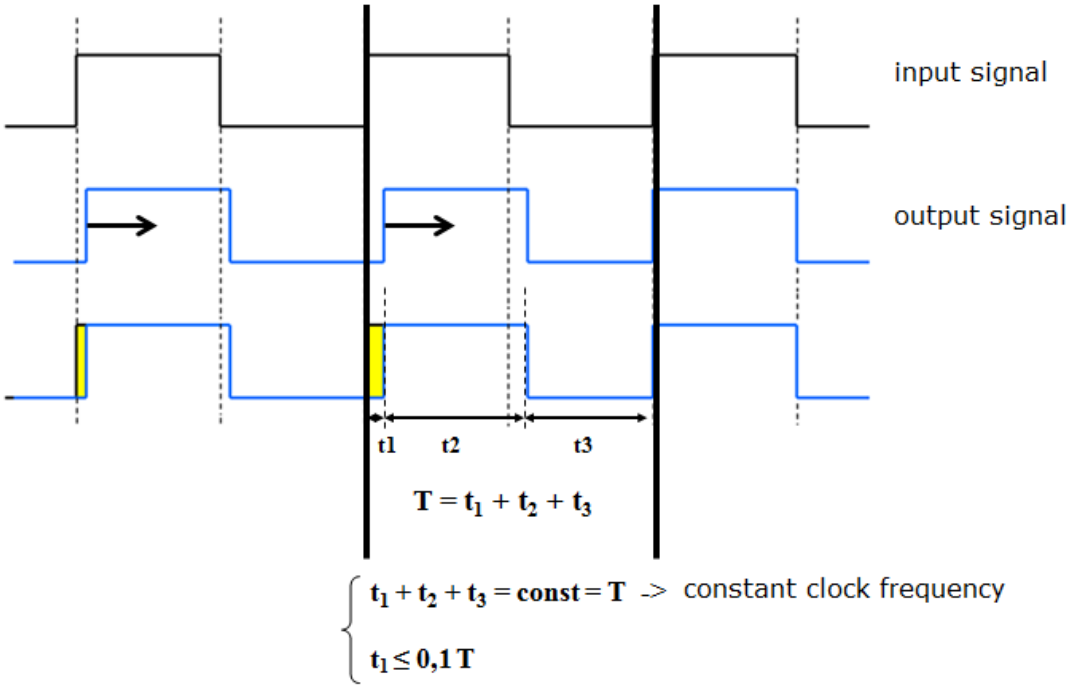

Figure 2.13. Jitter generator functioning schema

In Figure 2.14 the principal structure of a jitter generator is presented. Similar approach has been described in a U.S Patent [12]. However, neither of those works presents a solution that can be directly described in a VHDL code due to lack of analysis in that direction.

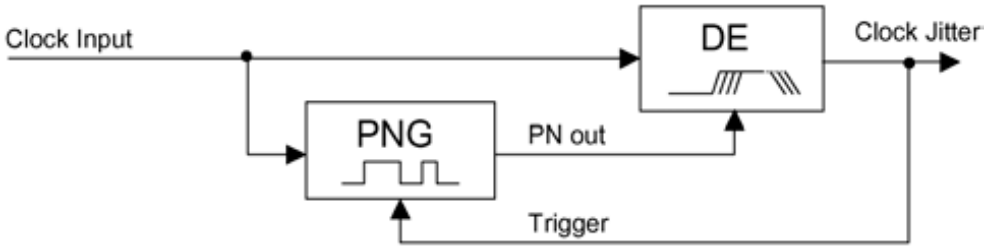

Figure 2.14. Principal structure of a jitter generator [1]

Generally, jitter consists of Pseudo Noise Generator (PNG) and Delay Element (DE). Pseudo noise generator is responsible for selecting relatively randomly a delay. The delays are created by a Delay Element that consists of propagating variously belated signal. However, triggering a Pseudo Noise Generator by an output clock of jitter generator is risky. The glitches can occur between two different cycles due to the lack of proper setup time of the Pseudo Noise Generator. A better way to handle this depends on adding an extra delay to the Delay Element. That delay would last longer than

a maximal possible jitter size. Thus, the Pseudo Noise Generator would have enough time to set properly its outputs before the next cycle of the clock input occurs. This approach is presented in details in Figure 2.17.

Table 2.1. First 19 polynomials of LFSRs

Bits n	**Feedback polynomial**	**Period** $2^n - 1$
4	$x^4 + x^3 + 1$	15
5	$x^5 + x^3 + 1$	31
6	$x^6 + x^5 + 1$	63
7	$x^7 + x^6 + 1$	127
8	$x^8 + x^6 + x^5 + x^4 + 1$	255
9	$x^9 + x^5 + 1$	511
10	$x^{10} + x^7 + 1$	1023
11	$x^{11} + x^9 + 1$	2047
12	$x^{12} + x^{11} + x^{10} + x^4 + 1$	4095
13	$x^{13} + x^{12} + x^{11} + x^8 + 1$	8191
14	$x^{14} + x^{13} + x^{12} + x^2 + 1$	16383
15	$x^{15} + x^{14} + 1$	32767
16	$x^{16} + x^{14} + x^{13} + x^{11} + 1$	65535
17	$x^{17} + x^{14} + 1$	131071
18	$x^{18} + x^{11} + 1$	262143
19	$x^{19} + x^{18} + x^{17} + x^{14} + 1$	524287

To build a digital jitter, a Linear Feedback Shift Registers (LFSR) can be utilized as a Pseudo Noise Generator [3]. Linear Feedback Shift Register is a shift register that generates pseudo-random sequences. It consists of generating a new input bit by applying a linear function to some of the previous states called taps. There are only two linear functions: ***xor*** and ***inverse-xor***. In LFSR the former one is commonly used. The initial state of LFSR is called seed. Seed is a sequence of bits in registers after a reset of a system. Because LFSR is deterministic, it is possible to determine the next and the previous state from the current set of bits. Therefore, it is recommended to use different seeds for jitter generator in order to avoid the same jitter size in each cycle. Moreover, the seed with all 0s is forbidden because the ***xor*** function would never generate

any other state then. It is possible to create both hardware and software versions of the LFSR.

The period of the LFSR depends on the number of bits it contains. It can be determined from the equation: $2^n - 1$, where *n* is a length of LFSR. LFSR feedback can depend on two or more taps as it is presented in table 2.1. There are two types of LFSR:

- **Fibonacci LFSR** – a new input bit is created by at least two taps. Signals from that taps are XORed and the value is placed in front of the shifter (Figure 2.15). The last bit disappears and all other bits are shifted to the right.

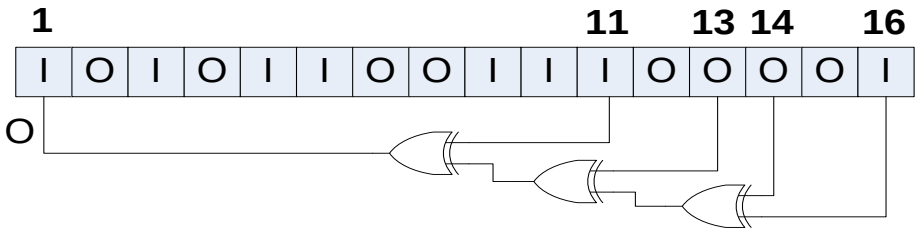

Figure 2.15. 16-bit Fibonacci LFSR. The feedback tap numbers correspond to a primitive polynomial in table 2.1. Hence, the register's maximum period equals to **65535** states excluding the all-zeroes state which is forbidden

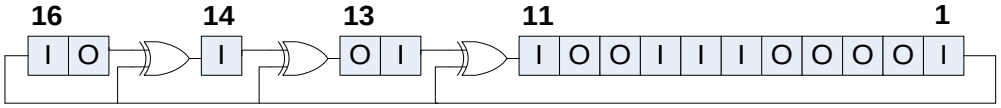

Figure 2.16. 16-bit Galois LFSR. The register numbers correspond to the same primitive polynomial as the Fibonacci instance in table 2.1. but are presented in reverse to the shifting direction. Here also the register's maximum period equals to 65535 states excluding the all-zeroes state which is forbidden

- Comparing to Fibonacci LFSR, in **Galois LFSRs** the taps are XORed with the output bit before they are placed in the next register (Figure 2.16). In particular, when an output bit is equal to "0", then all taps preserve their values. The register is only shifted to the right and the output bit "0" becomes a new input bit. On the other hand, when the output bit is "1", then all taps change their value

and the register is shifted to the right. The new input bit is “1”. Galois LFSR does not calculate each tap in order to produce a new input bit. Thus, it is faster and calculations can be processed in parallel reducing the propagation time.

The Galois LFSR is commonly used in digital circuits. However, for conducting research and simulations it does not matter which solution is chosen.

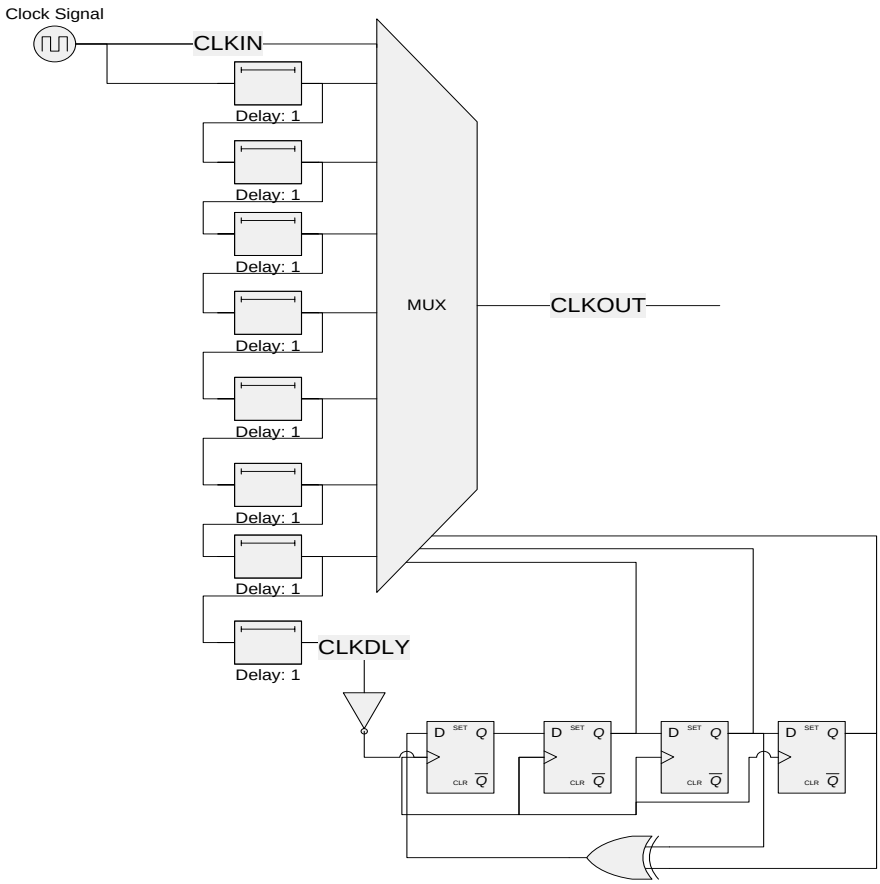

Figure 2.17. Sample jitter generator schema

In order to create a programmable Delay Element (DE) a chain of invertors or buffers can be utilized [12]. The whole solution for a reasonable jitter generator is presented in Figure 2.17. It consists of:

- Clock generator (input clock signal)
- Chain of delay elements (each contains two invertors)
- Multiplexer
- 4 bit LFSR

The aim of a multiplexer is to select an appropriate delay line that will be propagated to the output (CLKOUT). The LFSR is triggered by the last additionally delayed clock signal (CLKDLY) to avoid any metastability and glitches that could occur at the output of jitter. However, in order to speed up simulations and prevent recalculations of Delay Elements, a jitter generator available in the GALS EMI simulator was applied. It had no adverse effect on the final results.

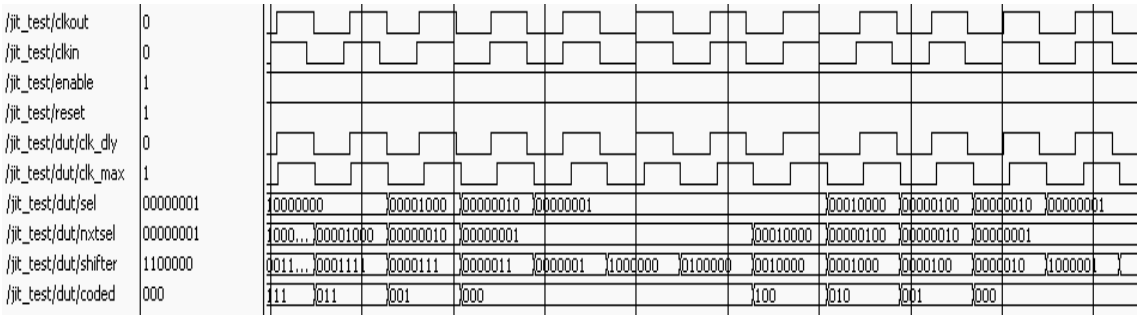

Figure 2.18. Behavioral simulation of a jitter generator

An outlook of a behavioral simulation of the jitter generator described before is presented in Figure 2.18. *Clk_max* (corresponding to CLKDLY signal in Figure 2.17) is a signal that triggers the LFSR. This signal has a maximum delay in order to prevent glitches occurring. Moreover, the LFSR is triggered when all the clock signal (input and output) are in the low state. Thus, there is enough time for registers to complete proper setup. The *Sel* signal represents a value of LFSR. Although it contains 4 bits, only 3 are used (the *coded* signal) in order to select 1 out of 8 delay lines that is propagated to the output. It can be clearly observed, that during each cycle, the delay of output clock is propagated according to the selected delay element.

In GALS systems with pausable clock only a jitter can be added to a system (to each GALS module). Integrating a phase shift would be a useless procedure. Phase shift is already present by the nature of the GALS methodology.

Table 2.2 presents the results of measurements of pseudo-random jitter generator at RTL level (register transfer level). They were determined by simulation, in order to obtain an accurate data about jitter to investigate its impact on the performance of the entire digital system [53]. The input clock was set at 100 MHz (10 ns cycle time). "Delay Line" means a line that has been selected in current cycle. In addition, individual

parameters were determined for each of the lines. The second column presents the delay between the transition of the input clock and the output from low to high state. Despite the fact that the delay is increased with the increase of the delay line, it is not linear. The difference between the two values is not constant and it is caused by various path lengths that go to multiplexer. However, it is assumed for further research, the average rate as 130 ps and it is equal to the propagation time of two connected inverters.

Table 2.2. Jitter generator – output signal delay

	Delay Line	**Delay (ps)**
MIN	00000001	207
delay	00000010	357
	00000100	479
	00001000	635
	00010000	751
	00100000	906
	01000000	1019
MAX	10000000	1175

It can be observed (Table 2.2) that using 100 MHz clock and 8-elements delay line, the maximum clock cycle reduction is 10%. This value is more than sufficient for our study, because in practice and in the literature there are no examples of a successful implementation of a synchronous system with higher jitter parameters. On the other hand, if 200 MHz clock source is used and 4 delay elements are applied, a 10% jitter is also created. The results would be similar with a slower clock source. Using a 50 MHz clock could increase the resolution of the generated fluctuations with the same delay elements (inverters) precision. It is also possible to replace the delay elements implemented as two connected inverters by using dedicated components (e.g. specially elongated tracks). It is assumed that the delay generated by such a construction would have shorter propagation time than two inverters in that technology. This would increase the resolution of jitter and its further ability to generate appropriate fluctuations at higher clock speeds.

2.4. GALS practical example in reducing EMI

In papers [22] and [23] a case study of implementing GALS technology in order to reduce EMI has been analyzed and presented. The work is based on a simulator described in this dissertation and developed by the author. GalsEmilator facilitated a process of selecting appropriate parameters of GALS system in order to maximize EMI reduction in such a circuit.

The investigated circuit consisted of 64-point GALS FFT processor divided into two cascaded 8-point FFT algorithms (Figure 2.19). The 8-point FFT was build with a novel Radix-23 FFT algorithm, which utilizes 3 stages of the butterfly (BF) structure. In that case and architecture, there was only one special twiddle factor multiplier necessary to build a pipelined 64-point FFT.

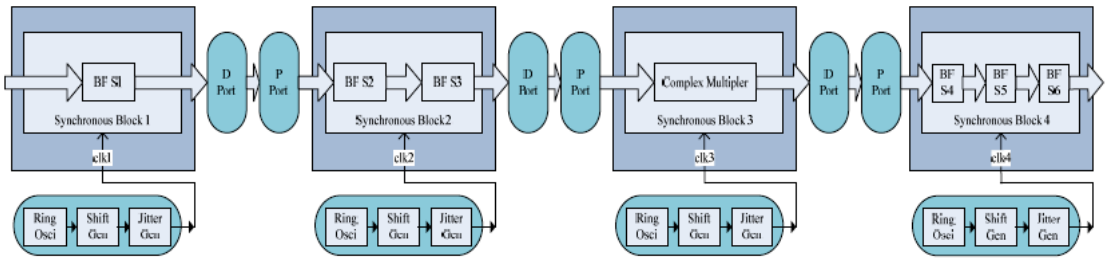

Figure 2.19. Block diagram of the GALS FFT processor [22]

As it is described in the paper [22], the authors designed the pausable clocking based GALS architecture (Figure 2.19) in order to reduce EMI (that is crucial for analog/digital circuits design) caused by simultaneous switching noise (SSN). It was necessary to develop special GALS connections between each block in order to support communication and data flow. For that reason, each synchronous block (there are 4 of them) is covered with an asynchronous wrapper. The asynchronous wrapper contains local clock generator and at least one asynchronous port (the middle blocks contain both I/O ports). Furthermore, each clock generator can be modulated. It was expected that such a modification of a regular chip design should reduce sharp peaks in the system supply current and finally the EMI of the whole system.

The 64-point FFT circuit was divided into seven functional sub-blocks in the pipelined processor. There are six butterfly structures and a complex multiplier. The sub-blocks have been arranged into four synchronous blocks according to their power

and current requirements. In order to establish the power consumption precisely, the authors prepared dynamic power analysis using simulation waveforms of the synthesized netlist in the IHP 0.13µm CMOS standard cells library technology. Table 2.3 shows the results of arranging the sub-blocks of the GALS FFT chip into four synchronous blocks. The blocks have similar power and current consumption.

Table 2.3. GALS FFT circuit partition according to power and current consumption [22]

	Sync. Block 1	Sync. Block 2	Sync. Block 3	Sync. Block 4
Function	BF Stage 1	BF Stage 2/3	Complex Mult.	BF Stage 4/5/6
Area (1)	38556µm^2	46119 µm^2	47459 µm^2	40547 µm^2
Number of FF	651	637	173	362
Average power (2)	1.2mW	1.5mW	1.2mW	1.7mW
Average current	1mA	1.25mA	1mA	1.4mA

Note: (1) Reported by Synopsys DesignCompiler;

(2) Reported by Synopsys PrimeTime at 80MHz working frequency.

In this work, two techniques were applied to the pausable local clock generators in order to modify the clocks of each synchronous sub-block: phase modulation and frequency modulation.

Figure 2.20. Current profiles of four synchronous GALS FFT blocks with phase modulation [22]

Phase Modulation – local clock generators' signals are first propagated through a programmable delay line. Therefore, the rising edge of each synchronous block's clock can be shifted independently. This modification leads to diversification in time of synchronous blocks' switching activities. Moreover, it allowed reducing sharp peaks of

the whole system supply current by spreading them over the whole period. In that research the clock signals of each synchronous block has been shifted evenly among clock period. These parameters are presented in Table 2.4. The results of such a modification are shown on a simulation in Figure 2.20 where a phase shift has been applied to each synchronous GALS block.

Table 2.4. Phase modulation of each clock generator among synchronous blocks [22]

	Sync. Block 1	Sync. Block 2	Sync. Block 3	Sync. Block 4
$t_{CLK}+$	0	$T_{CLK}/4$	$T_{CLK}/2$	$3T_{CLK}/4$

This technique is also applied to traditional synchronous designs as it was stated before, in order to spread switching activities of the processor. It allows designers to modify a shape of current supply in digital circuits. They can adjust both clock latency as well as clock skew in the global clock tree network. However, this modification is restricted by a synchronous design where limits are applied to setup-time and hold-time of the circuit. Therefore, only up to several percent of clock period the clock phase modulation can change. On the other hand, there is GALS design where asynchronous ports let the whole system to work with independent clocking systems. Thus, the parts of the system can work with a clock shifted even 50% of the base clock period. GALS technology enable digital circuit designers to overcome limits imposed by a synchronous design and apply phase shift to each GALS block without restrictions.

Frequency modulation – jittered clock signal; the second approach to minimize EMI and reduce SSN is to introduce a quick frequency modulation – clock jitter. It spreads the supply current in spectrum. The authors of the GALS FFT system added that feature to their design. Figure 2.21 and 2.22 present a jitter generator model and its clock period variations. The input clock signal is propagated through a delay line which is built of a chain of delay elements. The output signal delay depends on the line selected by a multiplexer. There are various ways to control the multiplexer and thus generating delayed signal. It can be either liner or randomized in terms of selecting delay and further modulation of the input signal. In both cases designers should focus

their attention on avoiding glitches on the output clock, which could have a detrimental effect on whole GALS system.

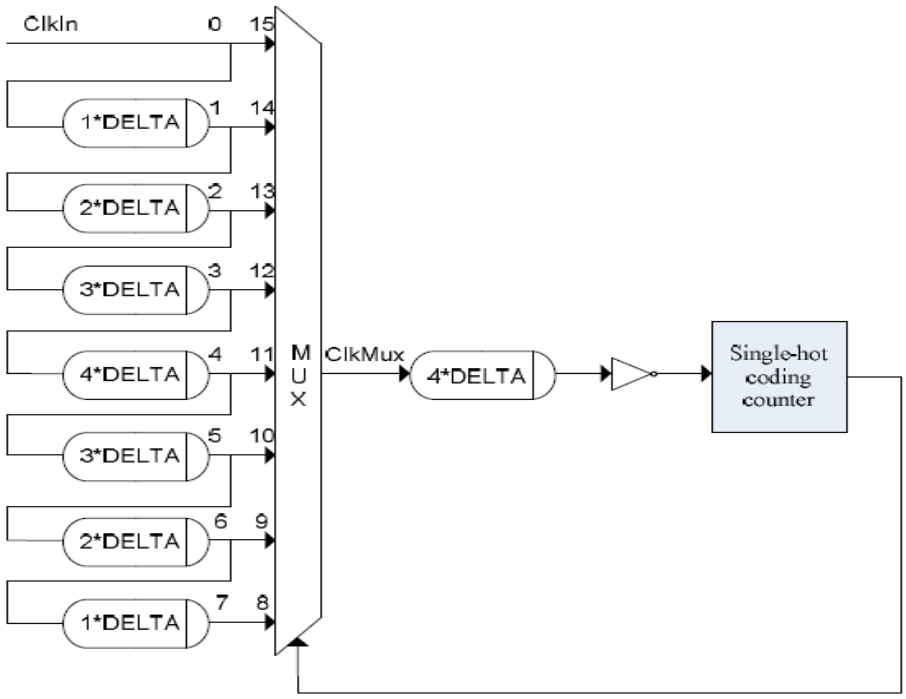

Figure 2.21. Jitter generator schema in GALS FFT digital circuit [22]

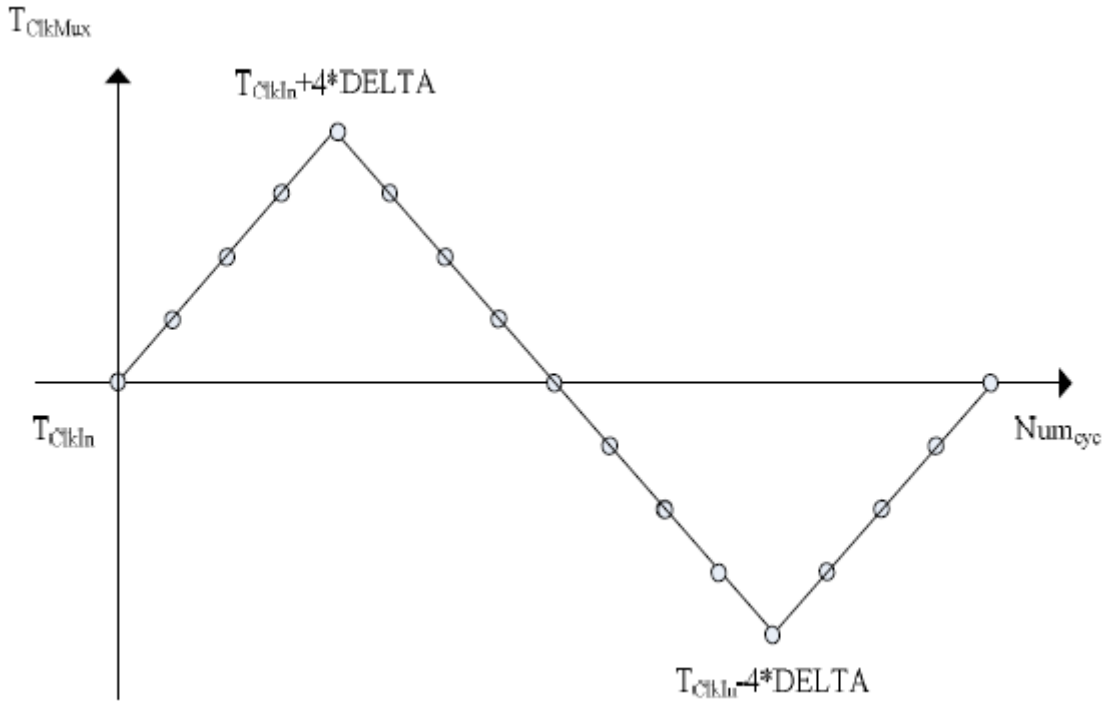

Figure 2.22. Triangular modulation of clock frequency in GALS FFT digital circuit [22]

The authors of the GALS FFT systems have utilized a single-hot coding to modulate the output clock in a linear mode. In that case, the clock period T_{CLK} alters from T_{CLK}-*4DELTA* up to T_{CLK}+*4DELTA,* where DELTA determines modulating granularity and is equal to 0,15ns. Moreover, the four local clocks are initialized with different offsets on T_{CLK} in order to improve randomization of the whole system clocks' signals.

In order to verify the designed GALS FFT system and compare its parameters regarding EMI/SSN with its synchronous counterpart, a GalsEmilator has been utilized. Details about system fragmentation, clock frequencies and their modulations of each block, maximal current requirements of each synchronous block were used in the program to generate current profiles of the systems. Afterwards, a current supply spectrum of both systems has been compared in a range from 0 to 20GHz (Figure 2.23). It is clear that the attenuation in GALS design averages around 10 dB in frequency domain comparing to the synchronous approach. It allowed the assumption that by utilizing clock modulation and system portioning, SSN can be reduced significantly and thus EMI in the digital circuit. Further investigations confirmed that the simulations results are true in terms of real chip testing.

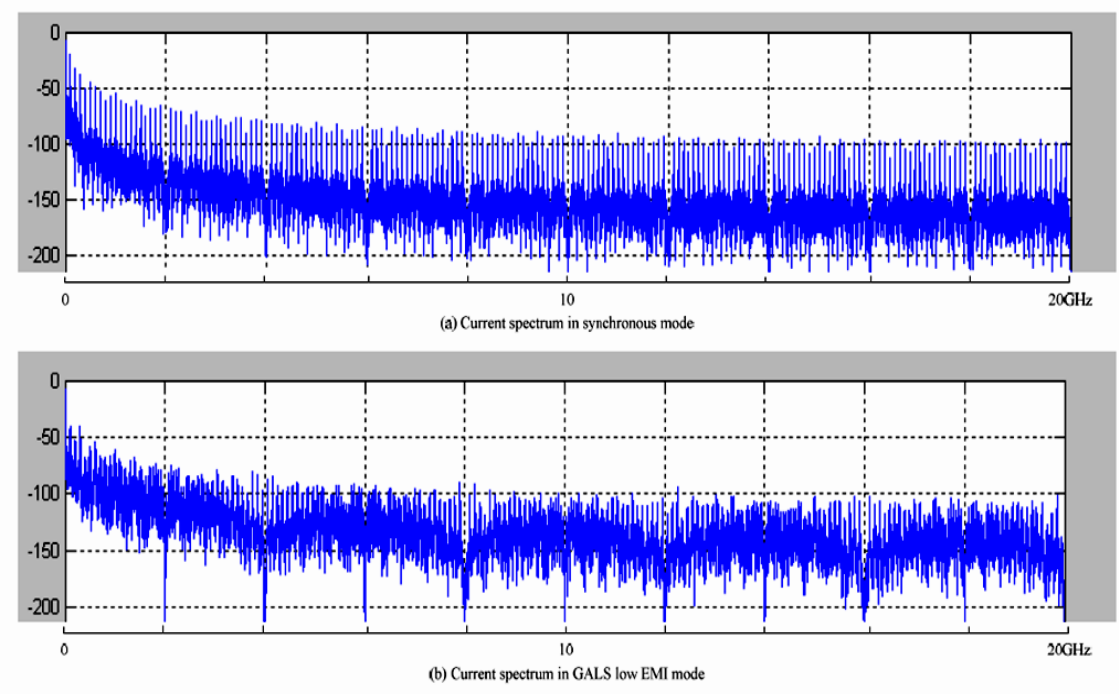

Figure 2.23. Comparison of current spectrum of synchronous mode and GALS low-EMI mode with MATLAB simulation in GalsEmilator

The described 64-point FFT processor was fabricated in the IHP (Institute for High Performance Microelectronics, Frankfurt, Oder). 0.13µm-1.2v six fold-metal standard CMOS technology [22]. The die size is 1730 µm x 1730 µm with 52 IO pads, as it is presented in Figure 2.24. Next, the chip was placed in a 64-pin PQFP, and the final product was successfully tested and measured in terms of its electric and EMI characteristic in IHP.

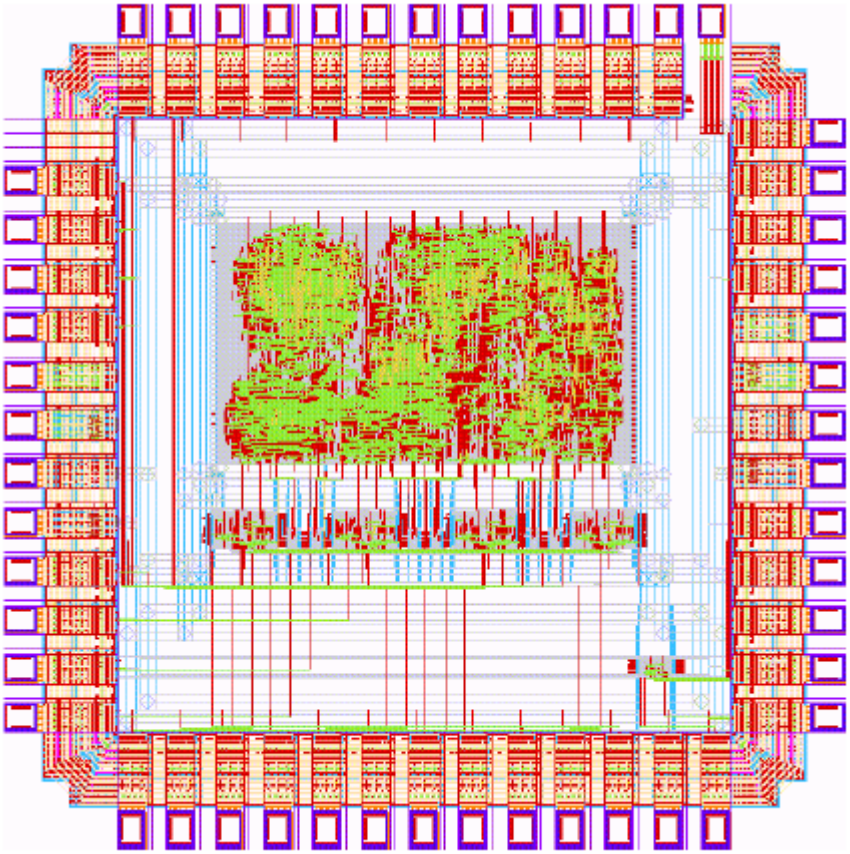

Figure 2.24. Die micrograph of the tested GALS FFT processor [22]

The supply voltage (V_{dd}) of the produced chip has been measured in frequency domain against different working modes. The results are presented in Figures 2.25, 2.26, 2.27, 2.28. Moreover, the corresponding attenuation of the spectral peaks has been shown in Figure 2.29.

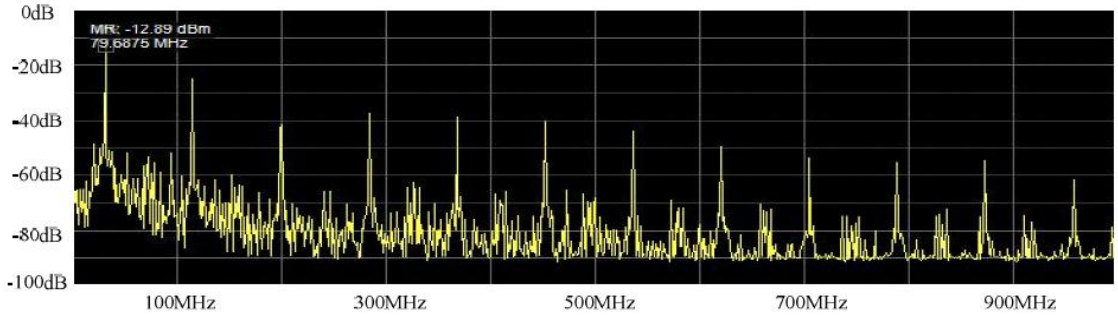

Figure 2.25. V_{dd} spectral analysis of the produced GALS FFT working in Synchronous mode [22]

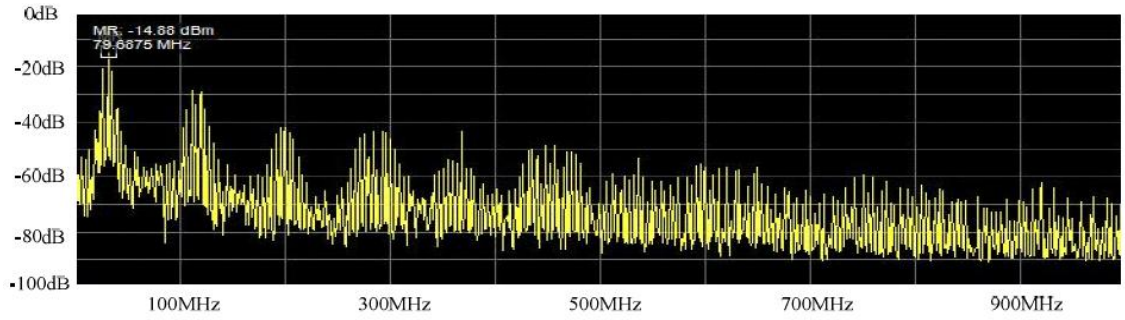

Figure 2.26. V_{dd} spectral analysis of the produced GALS FFT working in Synchronous mode with clock jitter [22]

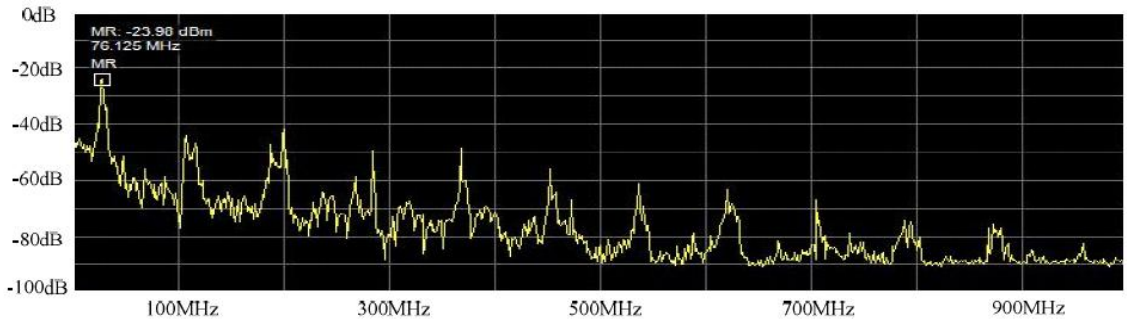

Figure 2.27. V_{dd} spectral analysis of the produced GALS FFT working in GALS mode [22]

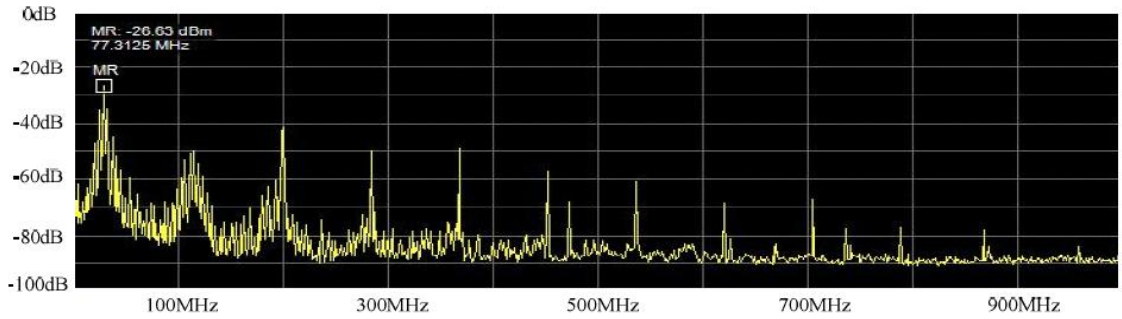

Figure 2.28. V_{dd} spectral analysis of the produced GALS FFT working in GALS mode with clock jitter [22]

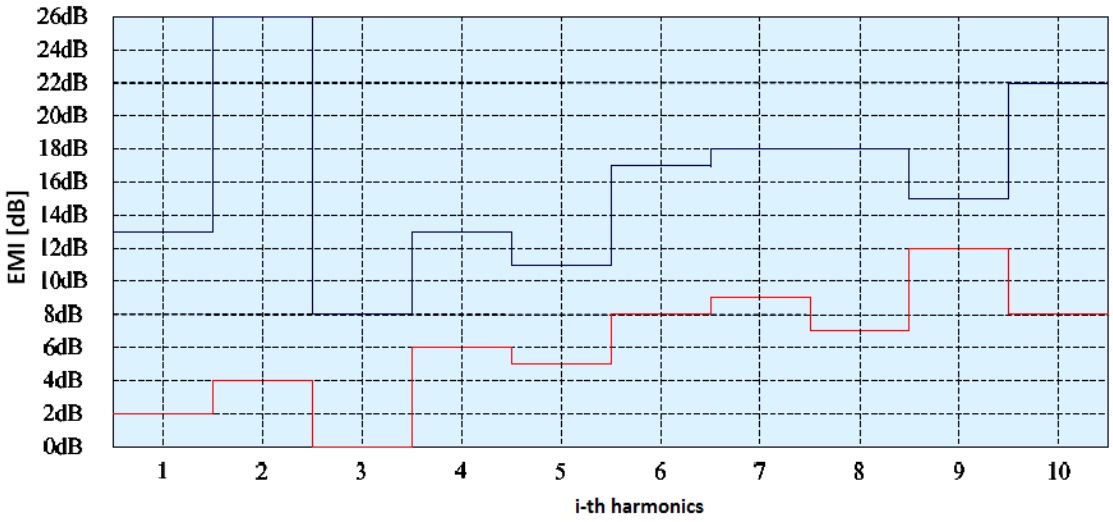

Figure 2.29. EMI reduction in the spectral peaks of i-th harmonics in the tested GALS FFT system. **Red line** – synchronous mode with jittered clock; **Blue line**: GALS mode with jittered clock [22]

The results confirmed that presented further in this dissertation simulator is fully functional. It can be seen from the Figure 2.29 that even a relatively simple GALS system reduces EMI significantly in comparison to its synchronous counterpart (11dB of the main peak). Moreover, according to simulations and real-life tests, jitter added to a clock generator reduces EMI further, mainly among higher harmonics. This confirms a significant match between simulations of the model and actual chip behavior. Simulated gain was around 10,5 – 11 dB and the measured one was equal to 11dB. The model was run with a limited data, where usually an approximate shape of a current in every

block is necessary to achieve better results. However, even without the data, calculations showed were an adequate prediction.

3. Modeling EMI in digital systems

In this chapter, GALS EMI simulator and GALS modeling approach with hybrid algorithm are presented. First, the developed software tool is described in details. Next, several GALS topologies are explained. Additionally, three different data transfer scenarios are demonstrated in GALS systems. Finally, system's parameters utilized for simulations and hybrid optimization are explained briefly.

3.1. GALS EMI simulator

In order to investigate EMI characteristic in the digital circuits caused by the digital clock behavior, a dedicated software tool called "GalsEmilator" has been developed. GalsEmilator (Figure 3.1) is a program created in Matlab in order to investigate EMI in various types and topologies of GALS systems (including synchronous solutions). It contains a number of options to model, as precisely as possible, the parameters of each GALS/synchronous system. Hence, it is feasible to observe the noise behavior in frequency and time domain simultaneously.

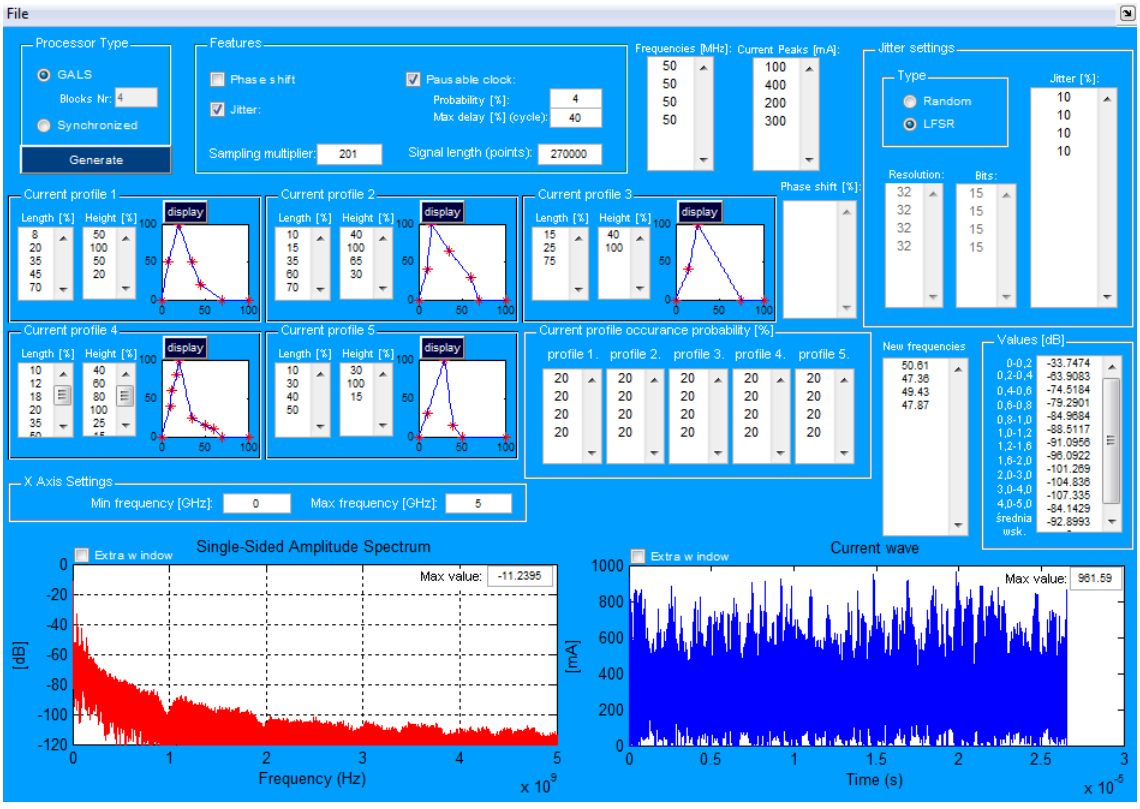

Figure 3.1. GalsEmilator – software to model EMI in synchronous and GALS systems

In the developed tool, main focus was to enable modeling different current shapes for different clock cycles. The software allows describing up to five different current profiles and specifying the probability of their appearance in the system.

For each block of the synchronous system, a clock phase shift (in respect to the global clock frequency) and additional jitter can be also set. For GALS modules, we can model extra clock jitter and also model pausable clocking [8] as a dominant technique for low-EMI GALS circuits. A model of GALS with pausable clocking allows us to simulate GALS wrappers that can pause the clock in order to perform a handshake operation. This behavior can be modeled by setting a probability of pause occurrence and a maximum delay of the pause. The delay is variable and, therefore, in our model it is randomized.

All simulated results, as shown in Figure 3.1, can be observed and analyzed both graphically and in generated tables. The complete software has its own user-friendly GUI.

3.1.1. Simulator description

Figure 3.2 presents an UML activity diagram for GalsEmilator. It shows the way in which the software should be handled properly. All actions to run a successful simulation are presented step by step. The simplified model of GalsEmilator algorithm is presented in Figure 3.3.

First of all, it is possible to select, in the simulator GUI, a chip type. There are two previously described designs: GALS or Synchronous approach. After selecting a synchronous system it is impossible to select several options that are intended for GALS system e.g. “pausable clock”. Moreover, in GALS system, each sub block’s frequency have to be specified, whereas in synchronous system only one is necessary.

Up to five current profiles can be described in the GUI by specifying their shapes in percentage. Hence, every current shape will be recalculated according to block’s frequency and sampling frequency creating a matrix of values for every block. Moreover, it is necessary to specify current shape occurrence probability for each of the blocks. The values determine how many times per 100 cycles every shape is going to occur. Usually, the equally distributed numbers are placed as it is difficult to define real figures within testing environment.

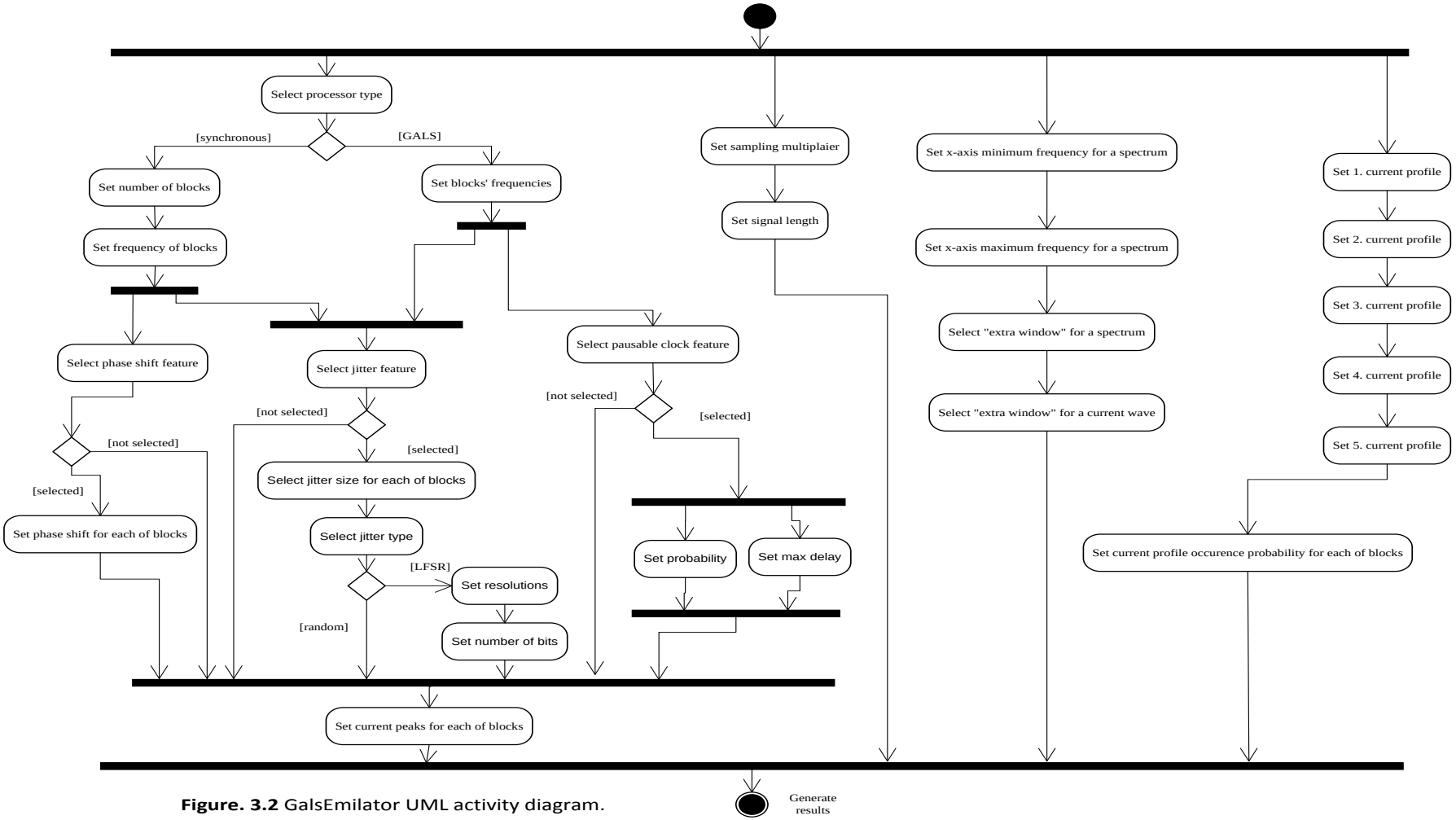

Figure. 3.2 GalsEmilator UML activity diagram.

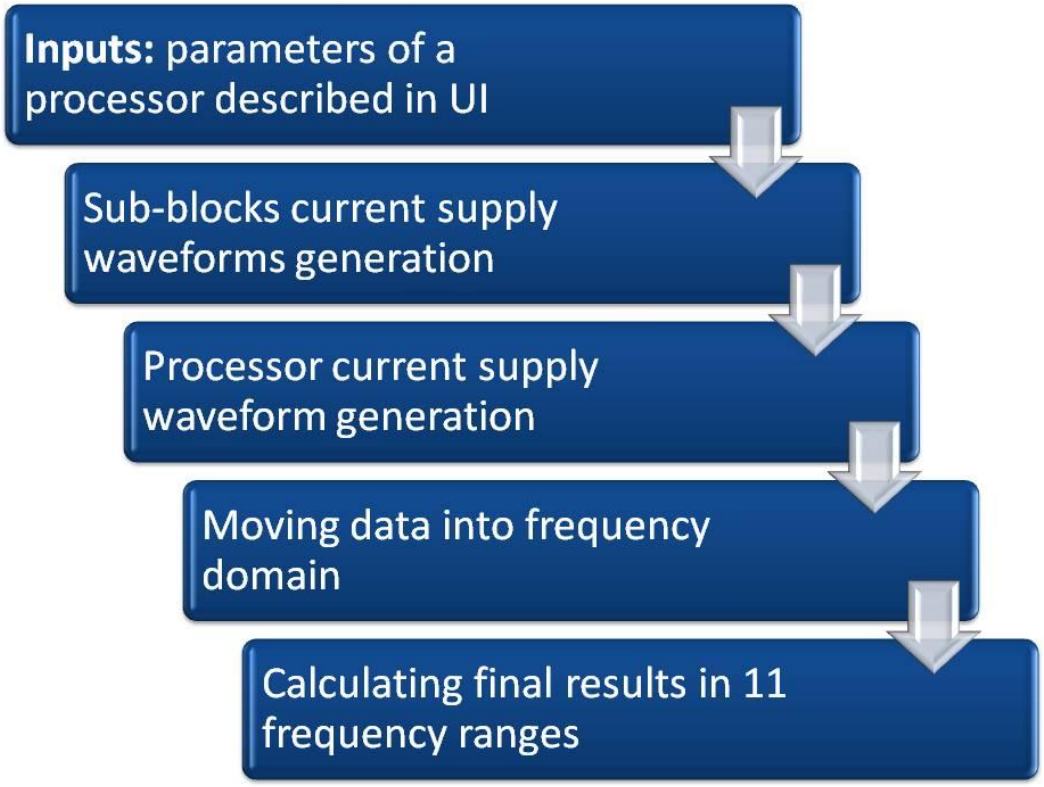

Figure 3.3. Simplified model description of GalsEmilator algorithm

Next, current waves for sub blocks are calculated in a time domain according to the blocks' frequencies, current profiles and their probability. Hence, the current waves are composed with a number of single patterns (Figure 3.4).

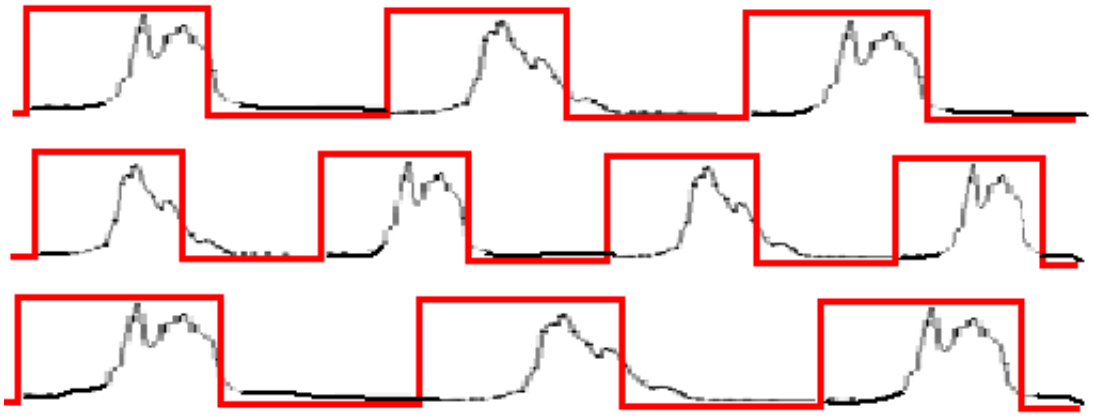

Figure 3.4. Sample clocking signals (red color) and corresponding current waves of GALS sub blocks. The simulator generates such waveforms in order to calculate a final wave composed of these sub-waveforms

At that moment there is one wave per block. Each wave can be additionally modified according to the features described later. Further, all waves are summed into one final wave of a whole chip. The FFT (Fast Fourier Transform) is used in order to move the final wave from the time domain into the frequency domain. After the transformation, it is possible to observe the whole spectrum and the EMI reduction in several ranges of frequency:

- 0,0 – 0,2 GHz (without 0,0)
- 0,2 – 0,4 GHz
- 0,4 – 0,6 GHz
- 0,6 – 0,8 GHz
- 0,8 – 1,0 GHz
- 1,0 - 1,2 GHz
- 1,2 – 1,6 GHz
- 1,6 – 2,0 GHz
- 2,0 – 3,0 GHz
- 3,0 – 4,0 GHz
- 4,0 – 5,0 GHz

The ranges were set according to the basic research frequency at 50 MHz and power corresponding to each of range. The higher range, the lower power it contains, so the range is wider. The ranges of spectrum in the lower frequencies are shorter because the values change more rapidly. On the other hand, in the higher frequencies the spectrum is flatter. Thus, the ranges can be relatively wider. Moreover, the ranges were set according to a case study (described before GALS FFT) that was investigated. The ranges can be easily scalable for different basic frequencies.

The result is only one value per range which indicates the highest value in the range (the noisiest frequency which is usually the *i*-th harmonics). The values (power) of a spectrum are presented in dB regarding the total current supply indicated as current peaks per each sub block, where A is an amplitude of *i*-th frequency (according to sampling frequency) in the spectrum, A_0 is total current supply (1A in this research):

$$L_{dB} = 10log_{10}\left(\frac{A^2}{A_0^2}\right) = 20log_{10}\left(\frac{A}{A_0}\right) \quad (3.1)$$

The second set of options that influences the way a waveform looks in each sub block are “Features”. It is possible to set:

- clock phase shift of each sub block (useful only with a synchronous design)
- jitter
- pausable clock (possible only for GALS systems)
- sampling multiplier
- signal length

Clock phase shift option contains additional text input box, where each shift of a block is defined in percentage. This feature moves a wave in time according to an indicated fraction (percentage) of its period. It can be useful when a mesochronous [40] system is investigated regarding EMI.

Jitter introduces a phase modulation (rapid phase fluctuations) to a waveform. It modifies slightly, up to the defined part of a period, the starting point of a rising edge, while the time of high level stays constant. Hence, jitter can increase or decrease frequency for one cycle but generally the base frequency remains unchanged. With the simulator GUI it is possible to select between random jitter, that uses the Matlab embedded random number generators (with the period of (2^19937-1)/2) and LFSR (Linear Feedback Shift Register). Selecting the LFSR method is necessary to specify also the LFSR length and the resolution of the delay chain. The LFSR length determines a number of bits used to create LFSR, thus the length of the period of a jitter is defined. The resolution of delay chain describes how many possible states of jitter will be applicable for an input clock signal.

Pausable clock option allows simulation of GALS wrappers that can stop a clock in order to confirm the handshake operation. It is necessary to specify occurrence probability of a pause and a maximum delay (fraction of a cycle). The delay length can vary in each step because it is randomized. The length that is specified indicates only the worst case scenario.

The two last options are focused indirectly on the whole final wave. Sampling multiplier describes how much faster would be the sampling frequency in comparison with the highest frequency of the blocks. It is suggested to remember that the lowest possible sampling frequency is twice the highest measured waves’ frequency (Nyquist–Shannon sampling theory). However, usage of the lowest sampling frequency is not

recommended because each cycle of the fastest sub block would be modeled only with 2 points. The suggested sampling multiplier is 200, although 100 would be also enough. The latter one is sufficient because the current shape of the fastest module will be modeled with 100 points which is usually enough to present every detail. However, the higher sampling multiplier the more adequate model but also the longer time of computations. The difference in results between those two sampling multipliers was insignificant but not every case had been investigated. Also the signal length that describes how long the modeled signal will be in points can be set.

It should be pointed out that each point of a waveform is calculated according to the sampling frequency. Generally, if there would appear a significant difference between two simulations, the signal length should be extended. It ought to reduce the variations between simulations with the same settings caused by several random values e.g. pausable clock or jitter generated by the Matlab random method. If the sampling frequency is too low, it might also be necessary to increase its value in order to improve results.

At the bottom of the GUI two small graphs are present. Although they are embedded into a GUI, there are extra options (checkboxes) that allow user creating the separate flexible charts. Then, all parameters of a chart can be modified. The latter graph shows a current wave in the time domain. The former displays the same wave in a frequency domain after Fast Fourier Transform. The values presented in the chart are compared with the sum of current peaks and presented in dB. Additionally, it is possible to specify the range of frequencies that will be displayed in a chart in order to investigate a fixed area. It facilitates the signals comparison and further evaluation.

3.2. Hybrid optimization algorithm

In order to investigate closely an influence of frequencies set against EMI reduction in GALS systems, it was necessary to design a hybrid optimization algorithm. The whole process is presented in Figure 3.5. Initial studies have been conducted which proved that the regular optimization algorithms are insufficient to give satisfactory results. It is because of the number of dimensions, which increase with the number of GALS modules, and irregular shape of the objective function with large number of local minimums. Therefore, a hybrid optimization shell was added to the GalsEmilator (Fig-

ure 3.5). The computational schema presented in the picture shows that there is a necessary number of GALS modules in the mode, modules' frequency ranges, jitter ranges or constant values, maximal current and its shape per GALS module to begin searching algorithm. As it was described before, the simulator calculates the results with initial parameters. Then, the parameters are changed according to hybrid optimization algorithm.

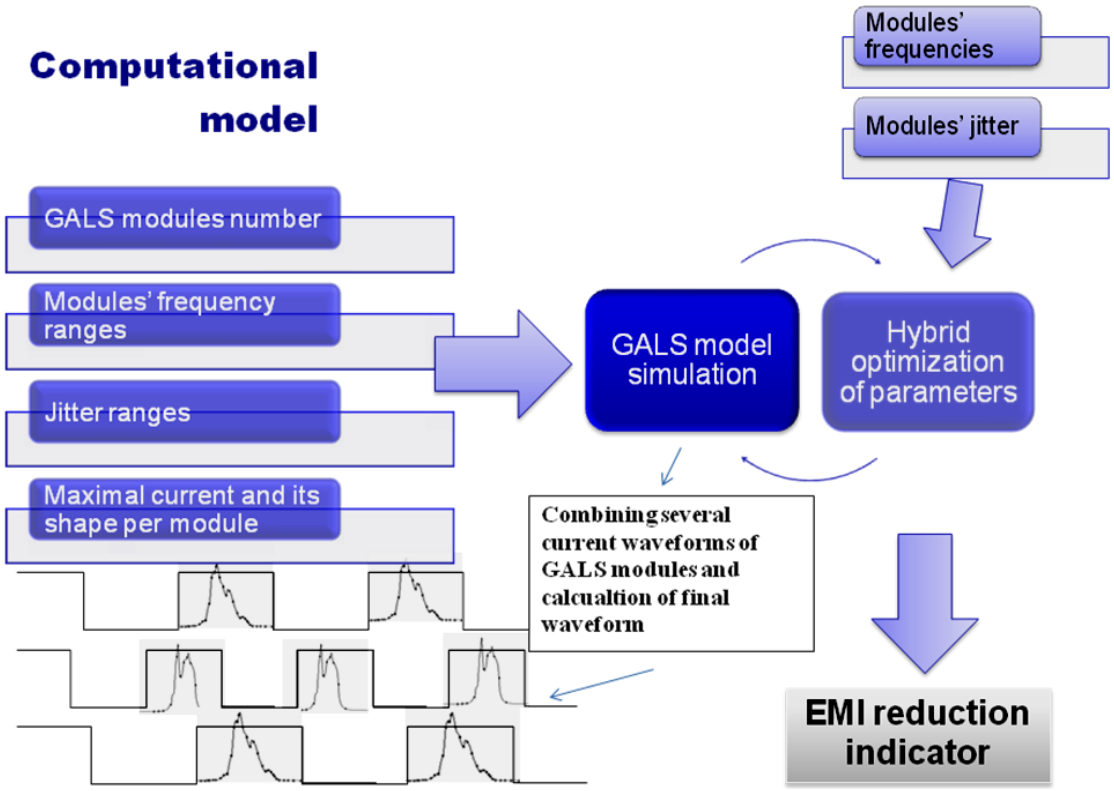

Figure 3.5. Computational model of hybrid optimization regarding EMI reduction in GALS systems

The objective function F is programmable, thus it can be either an average reduction of all ranges of investigated frequencies (there are used 11 range of frequencies from 0 to 5Ghz) or a special indicator where each reduction in a range has a rate (sum of rates is equal to 1):

$$F = 0,15r_1 + 0,14r_2 + 0,12r_3 + 0,11r_4 + 0,08r_5 + 0,08r_6 + \\ + 0,07r_7 + 0,07r_8 + 0,06r_9 + 0,06r_{10} + 0,06r_{11} \quad (3.2)$$

where r_i is maximal noise of EMI in each of 11 ranges described before. Corresponding numbers are factors of each of the ranges. The aim of hybrid optimization is to achieve a maximal reduction of EMI, it means F → min.

The objective function F should be chosen according to requirements and problem specification. For example when there is a need to attenuate EMI in low frequencies the factors can be set to focus only on that range and making the other ones obsolete. In this dissertation the average method has been utilized, however the presented indicator is also shown in results in order to illustrate the differences.

During optimization process two sequentially programmed algorithms are used (Figure 3.6). First of all, the Monte Carlo simulation is required to find the best global solution because there are many local minimums. According to the number of iterations and initial precision the algorithm runs in a loop.

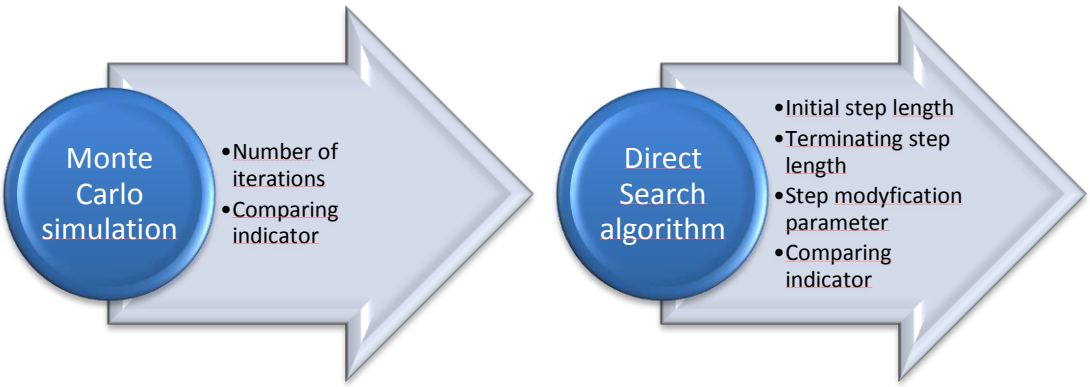

Figure 3.6. Hybrid optimization components and its parameters

When the Monte Carlo stage is finished, the best result is propagated to a second optimization algorithm – direct search algorithm (simple modification of Rosenbrock' method). It is powerful enough, no-gradient and relatively fast algorithm to improve the solution. It consists of searching better results among orthogonal vectors in a n-dimensional space according to number of GALS modules. The orthogonal

set of vectors is created according to rule where two vectors x and y are described in a unitary space X with scalar product {·,·}, where {x,y} = 0. The search can be also completed in an opposite direction to the orthogonal set. The initial step length is decreased when there are no better results until described value. A better result is checked among the set of vectors in every iteration. When it is found, the current point is moved to the best one in next step and the whole procedure is repeated. When there is no better solution, the step length is corrected accordingly to programmed value and the procedure is restarted. When the shortening of a step-length does not bring a better value and the step length is less than the required precision, the algorithm stops.

3.3. GALS modeling

The software was used to model and investigate EMI characteristics in different GALS and synchronous systems. For the GALS system, the focus was on the pausable clocking scheme that is very often used in contemporary GALS NoC systems [8], [9]. In order to accurately model the clock waveform of the GALS system, all evaluated systems have been described in VHDL and simulated. Next, the clock behavior is automatically extracted from the simulation conducted in ModelSim using the developed software tool. The second version of software was designed in order to facilitate this feature. Data is directly moved to the EMI simulator and evaluated. Such appendage of the software was needed to support exact matching to the real system behavior of the GALS interfaces. It was particularly challenging to extract clock behavior during the handshake process between the GALS blocks when clocks are paused, without access to real simulation data.

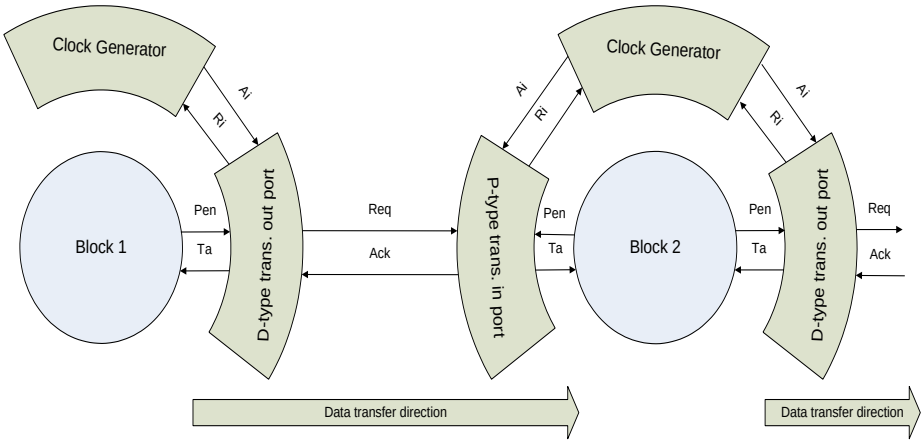

Figure 3.7. Sample of connection between two adjacent LS blocks used in models

In the **VHDL** (*Very High Speed Integrated Circuits Hardware Description Language*) models, the D-type output and P-type input GALS ports [7] have been used as shown in Figure 3.7. 'Demand Type' (D-type) ports pause the clock immediately after receiving request from the Locally Synchronous (LS) block. For the input side, 'Poll Type' (P-type) ports have been used. The standard 4-phase handshake operation between adjacent GALS modules was entirely modeled in the simulation.

3.3.1. Topologies of the evaluated GALS systems

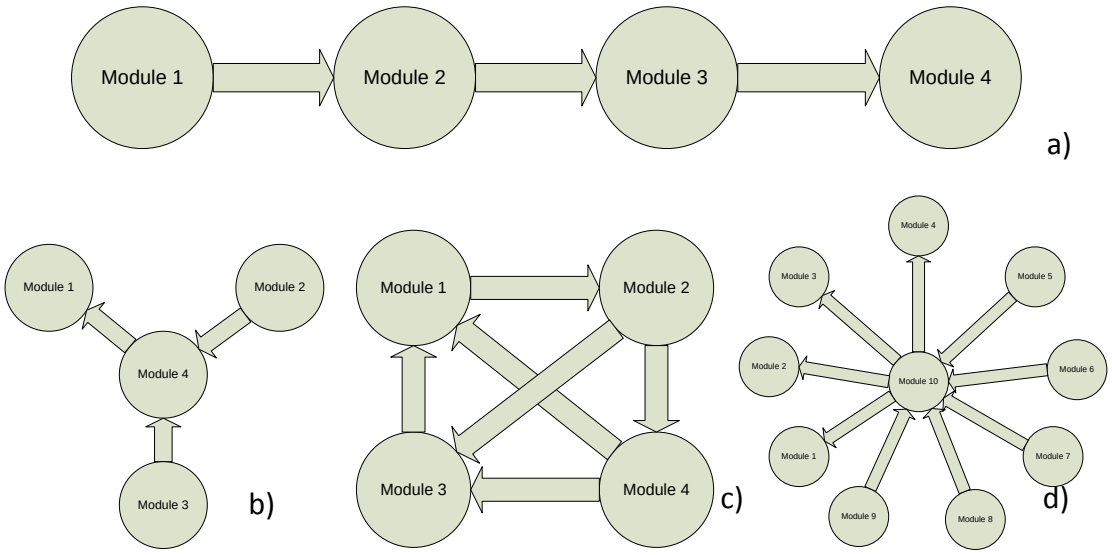

Figure 3.8. Various topologies of models: **a)** point-to-point **b)** star **c)** mesh **d)** large star

In evaluation four different structures of GALS circuits have been analyzed as shown in Figure 3.8. Different system topologies [38] have been investigated. Here, point-to-point (a), star (b) and mesh (c) topologies were taken into consideration. In order to check whether a granulation can influence the reduction of EMI, the star with a higher number of blocks (d) has been also examined. The goal was to evaluate different interconnect structures and to verify their impact on EMI in GALS systems. The arrow in Figure 3.8 indicates a direction of handshake and data transfer. In a point-to-point topology the direction is obvious. The modules have to be combined in a straight line where each module is connected with another one. In other topologies the direction of data transfer is rather unrestricted.

3.3.2 Data transfer scenarios

The outlook of the clock waveform varies significantly between different intensity of the data transfer since the clock pausing occurs only during the handshake process. For that reason, three different scenarios of the system behavior have been modeled:

A. Low data transfer, where the data transfer is performed relatively rarely (for instance, once per 6 clocks).
B. Medium-to-high data transfer, where half of the clock cycles are involved in data transfer.
C. Burst mode, where more than 80% of the clock cycles are data-transfer related.

Table 3.1. Patterns for low data transfer (A) for each designed topology

	4-module point-to-point, star	4-module mesh	10-module star
Pattern 1	100000	100000	100000
Pattern 2	000100	000010	000001
Pattern 3	000001	001000	001000
Pattern 4		000001	010000
Pattern 5		010000	000010
Pattern 6		000100	001000
Pattern 7			001000
Pattern 8			100000
Pattern 9			000100

Table 3.2. Patterns for medium data transfer (B) for each designed topology

	4-module point-to-point, star	4-module mesh	10-module star
Pattern 1	110100	010101	101010
Pattern 2	101010	111000	111000
Pattern 3	001110	001101	101100
Pattern 4		101100	001011
Pattern 5		000111	101010
Pattern 6		011100	000111
Pattern 7			100011
Pattern 8			101001
Pattern 9			011100

Table 3.3. Patterns for burst data transfer (C) for each designed topology

	4-module point-to-point, star	4-module mesh	10-module star
Pattern 1	110111	111011	011111
Pattern 2	011111	011111	111011
Pattern 3	111101	110111	111110
Pattern 4		111110	110111
Pattern 5		101111	011111
Pattern 6		111101	110111
Pattern 7			111110
Pattern 8			111011
Pattern 9			110111

In tables 3.1, 3.2, 3.3 the specific data transfer scenarios are presented. The sequence of bits indicates if the transfer occurs in a cycle or not. “1” means that a data transfer happens in a particular cycle, whereas “0” means no activity. Each pattern is handled by a Finite State Machine (FSM) that periodically selects bit-by-bit. Thus, it facilitates generating as long sequences as it is necessary for an extended simulation. Moreover, each pattern belongs to one-output port. For instance, the center block of the 10-module star contains 4 data transfer patterns.

3.3.3 Model parameters

For the system modeling purposes, a basic frequency has been defined which is an average of all other clock frequencies in the system. Such frequency was desired in order to compare a synchronous approach that usually includes just a single clock domain with a GALS system that is normally triggered by a number of different clocks. In the created model this basic frequency was 50 MHz.

GALS systems can be implemented in several ways. For instance, some systems can contain very similar clock frequencies for local blocks (plesiochronous clocking). On the other hand, different systems may have totally spread LS clock frequencies. Generally, 3 various frequencies' sets for modules have been utilized in the modeled GALS systems (Table 3.4 and 3.5). The first set represents plesiochronous (1) operation where the frequencies of each block are almost the same as the base frequency. In the second set (2), the difference is higher and in the third one (3), frequencies range up to a ratio of 1:3.

Table 3.4. Sets of frequencies utilized with 4-module GALS topologies in MHz

	plesiochronous (1)	medium differences (2)	high differences (3)
Module 1	49,5	45,45	100
Module 2	51,02	62,5	50
Module 3	50	50	33,33
Module 4	49,01	41,66	50

Table 3.5. Sets of frequencies utilized with 10-module GALS topologies in MHz

	plesiochronous (1)	medium differences (2)	high differences (3)	(4)	(5)
Module 1	49,02	41,67	83,33	71,43	71,43
Module 2	48,08	35,71	90,91	55,56	55,56
Module 3	47,17	55,56	100,00	35,71	35,71
Module 4	51,02	71,43	31,25	41,67	41,67
Module 5	52,08	33,33	33,33	33,33	83,33
Module 6	53,19	45,45	100,00	62,50	62,50
Module 7	49,02	38,46	83,33	38,46	38,46
Module 8	47,17	62,50	33,33	45,45	45,45
Module 9	46,30	83,33	35,71	50,00	50,00
Center module	50,00	50,00	50,00	83,33	33,33

There are also differences between models with different slower and faster blocks in respect to a clock frequency. For instance, in the star topology, if the center block is the fastest one, the whole system works more efficient. For that reason, 10-module star topology has been investigated with both slow and fast case (Table 3.5).

In all cases 10 GHz sampling frequency is used. This sampling is quite sufficient for the systems that were modeled since the current profile with 50 MHz clock was represented by 200 points in simulation. In this model, equal probability of occurrence for each of the five modeled current shapes was used. Also, the same jitter settings for

each simulation have been used, with the LFSR length of 15 bits and 32 delay elements. The sum of the current peaks in all cases was the same in order to correctly compare results. In the 4-module systems, the peaks were defined as:

- 100 mA
- 400 mA
- 200 mA
- 300 mA

In the 10-module systems distribution was the following:

- 2 x 200 mA
- 4 x 100 mA
- 4 x 50 mA.

For all simulations 5 current profiles with equal distribution for each block were used in simulations Figures 3.9, 3.10, 3.11, 3.12, 3.13.

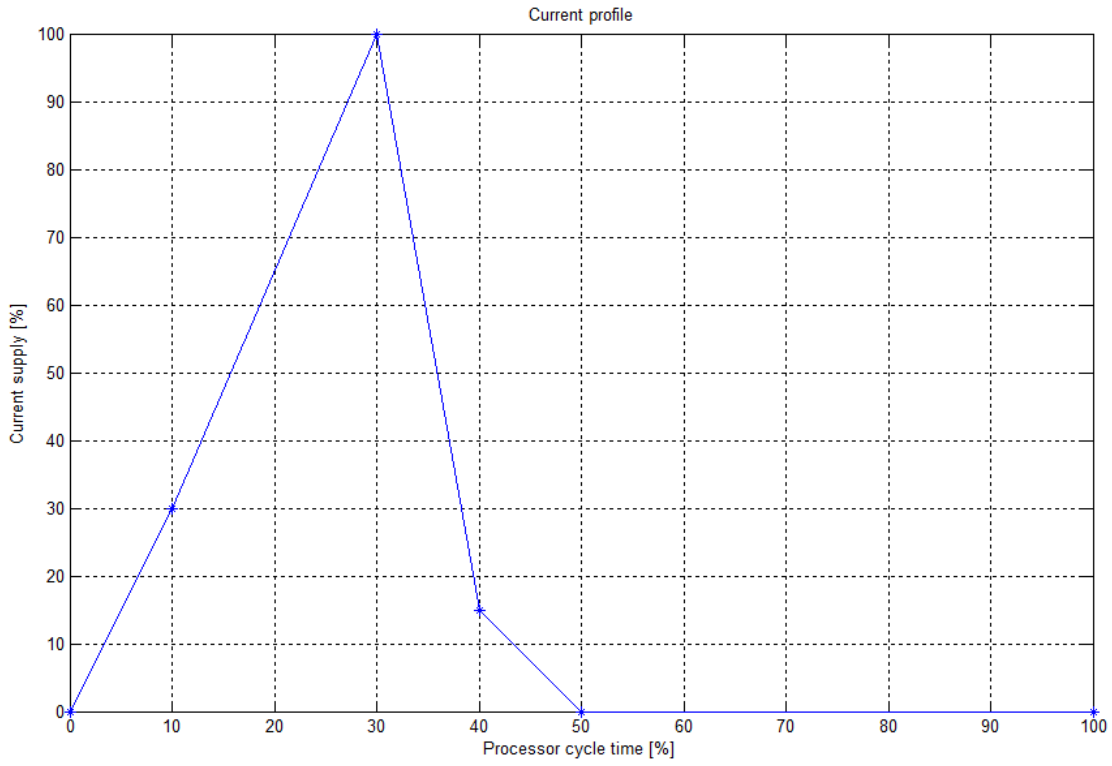

Figure 3.9. Sample current profile 1

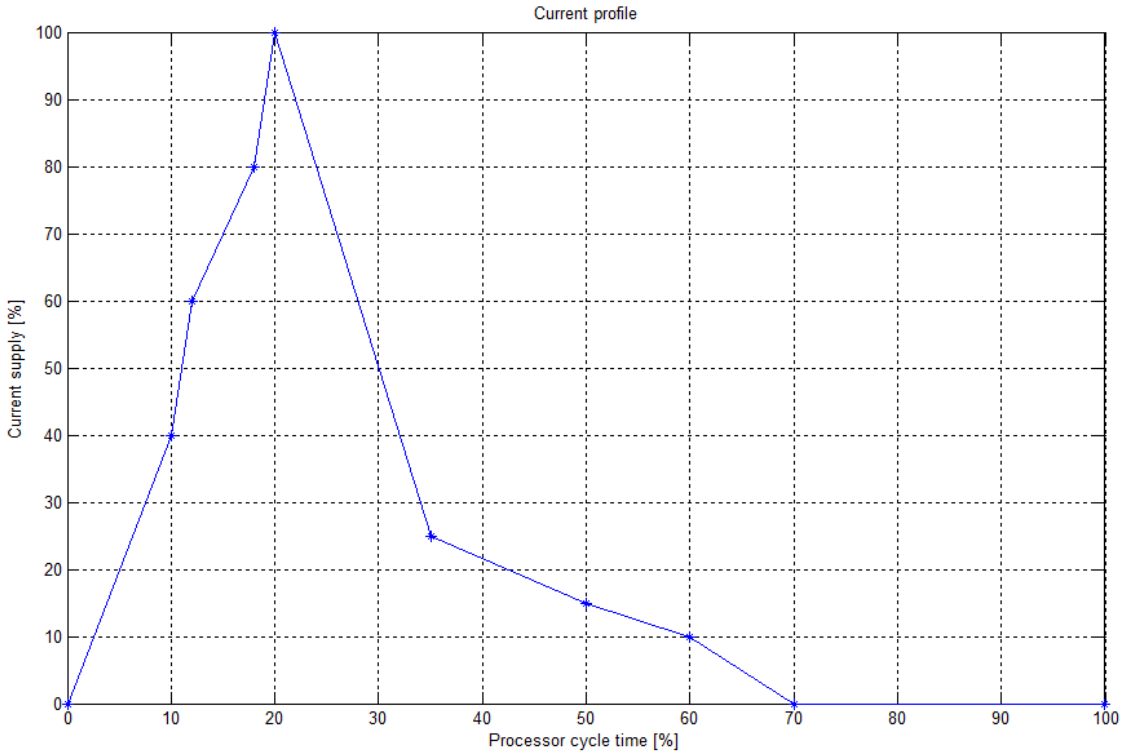

Figure 3.10. Sample current profile 2

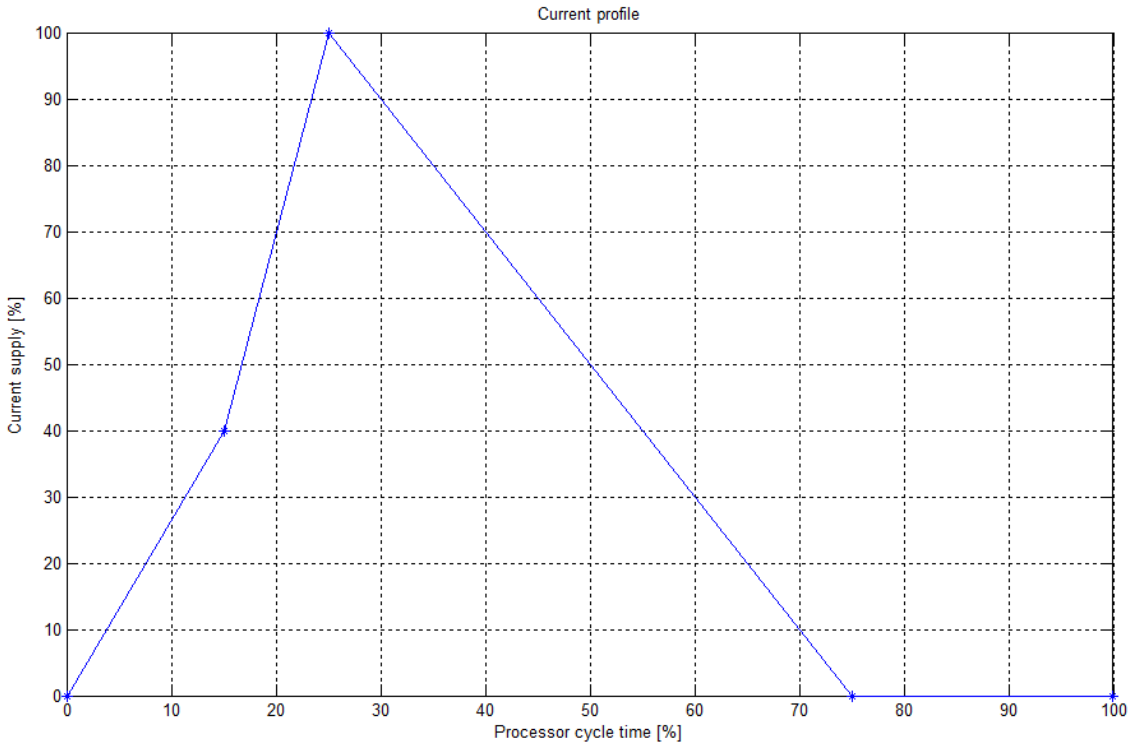

Figure 3.11. Sample current profile 3

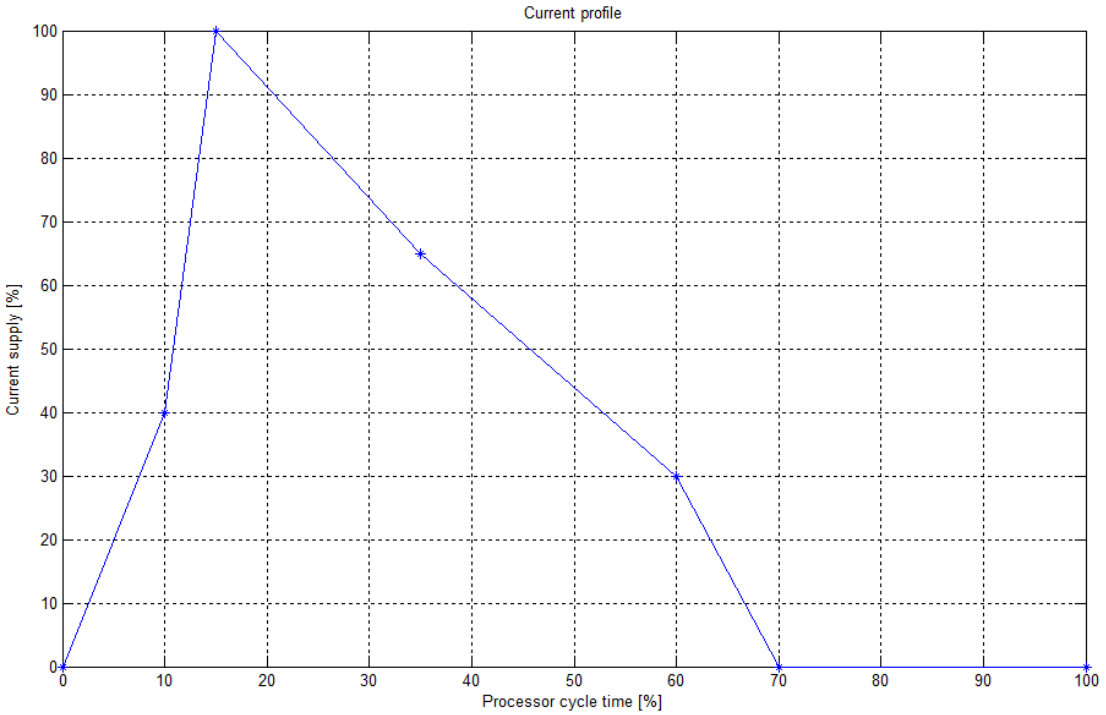

Figure 3.12. Sample current profile 4

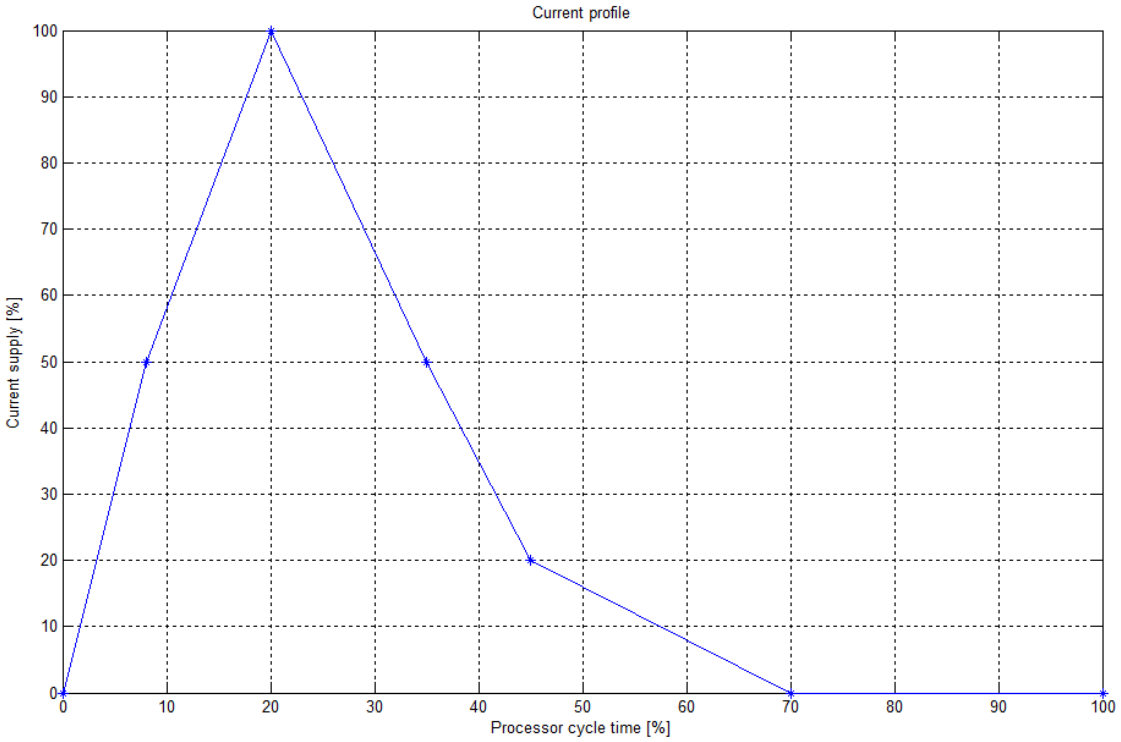

Figure 3.13. Sample current profile 5

4. Investigations and experimental results

This chapter presents the results of simulations conducted in “GalsEmilator” with different GALS topologies and settings. First, the values of synchronous system are presented. Then, the test records for GALS systems are described. The comparison between synchronous and GALS systems is shown. Finally results of automated method with **hybrid optimization** are presented. Results from investigations regarding synchronous system are treated as a source of reference for further investigations (***benchmark***).

4.1. Synchronous systems

Tables 4.1, 4.2 and 4.3 present detailed results of simulations for synchronous 4-module and 10-module systems with different features. As mentioned before, the synchronous systems have been modeled with different granularity, phase shift per module and clock jitter. The results are presented in dB and 11 frequency ranges. The aim of testing the synchronous approach was to obtain a comparable data that can be confronted with its GALS counterparts. It can be noticed that each feature applied to a synchronous system reduces EMI in a power spectrum. The range of reduction is strongly correlated with the settings of features.

Table 4.1. Results of simulations for the 4-module synchronous system with and without jitter, with different sets of phase shift per each module

Simulation number		1	2	3	4	5	6
Parameters	Phase Shift [%] per module	0	0	0	0	0	0
		0	0	25	10	25	10
		0	0	50	20	50	20
		0	0	75	30	75	30
	Jitter	no	yes	no	no	yes	yes
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-19,266	-20,911	-38,326	-26,955	-37,013	-28,956
	0,2 - 0,4	-50,995	-50,961	-50,611	-57,427	-51,096	-59,151
	0,4 - 0,6	-60,040	-71,238	-59,456	-64,011	-71,909	-78,081
	0,6 - 0,8	-62,290	-75,838	-63,504	-69,757	-79,454	-80,120
	0,8 - 1,0	-63,447	-81,782	-70,576	-69,803	-85,667	-85,040
	1,0 - 1,2	-66,817	-85,797	-74,782	-73,943	-89,179	-89,896
	1,2 - 1,6	-72,299	-89,600	-72,439	-76,089	-89,468	-91,792
	1,6 - 2,0	-75,947	-92,372	-82,053	-77,902	-95,816	-96,143
	2,0 - 3,0	-80,009	-95,863	-87,967	-86,892	-101,444	-102,396
	3,0 - 4,0	-83,066	-97,496	-87,387	-87,952	-103,999	-102,210
	4,0 - 5,0	-86,643	-101,018	-91,662	-91,776	-105,797	-105,717

Table 4.2. Results of simulations for the 10-module synchronous system without jitter and with different sets of phase shift per each module

Simulation number		1	2	3	4	5	6
Parameters	Phase Shift [%] per module	0	0	0	0	0	0
		0	10	15	50	5	60
		0	20	30	20	10	20
		0	30	45	40	15	40
		0	40	55	70	20	75
		0	50	65	90	25	90
		0	60	75	10	30	10
		0	70	85	30	35	30
		0	80	90	60	40	50
		0	90	95	80	45	70
	Jitter	No	No	No	No	No	No
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-19,278	-33,041	-35,070	-42,044	-26,955	-36,794
	0,2 - 0,4	-51,274	-67,965	-58,918	-61,637	-64,110	-65,274
	0,4 - 0,6	-59,970	-68,189	-68,639	-68,274	-75,435	-68,269
	0,6 - 0,8	-62,390	-79,134	-67,663	-75,408	-77,665	-71,965
	0,8 - 1,0	-63,611	-76,339	-76,843	-76,737	-70,948	-78,316
	1,0 - 1,2	-66,955	-85,213	-81,802	-82,516	-76,458	-78,853
	1,2 - 1,6	-72,674	-81,339	-82,537	-81,193	-90,063	-82,046
	1,6 - 2,0	-76,151	-84,173	-83,701	-87,209	-79,243	-86,272
	2,0 - 3,0	-80,085	-88,758	-89,020	-89,372	-89,077	-88,846
	3,0 - 4,0	-83,193	-93,482	-91,448	-95,889	-90,218	-93,130
	4,0 - 5,0	-86,707	-96,920	-93,799	-96,049	-97,077	-96,247

Table 4.3. Results of simulations for the 10-module synchronous system with jitter and different sets of phase shift per each module

Simulation number		1	2	3	4	5	6
Parameters	Phase Shift [%] per module	0	0	0	0	0	0
		0	10	15	50	5	60
		0	20	30	20	10	20
		0	30	45	40	15	40
		0	40	55	70	20	75
		0	50	65	90	25	90
		0	60	75	10	30	10
		0	70	85	30	35	30
		0	80	90	60	40	50
		0	90	95	80	45	70
	Jitter	Yes	Yes	Yes	Yes	Yes	Yes
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-20,901	-34,635	-36,376	-44,060	-28,874	-36,676
	0,2 - 0,4	-51,404	-70,979	-65,346	-62,629	-63,603	-69,739
	0,4 - 0,6	-71,022	-81,382	-79,825	-80,151	-81,716	-78,909
	0,6 - 0,8	-76,858	-84,816	-80,273	-84,584	-85,068	-85,429
	0,8 - 1,0	-83,644	-89,221	-85,644	-88,150	-87,576	-88,943
	1,0 - 1,2	-87,615	-91,213	-91,230	-92,167	-92,272	-91,347
	1,2 - 1,6	-93,427	-94,838	-94,941	-94,052	-95,064	-95,376
	1,6 - 2,0	-97,266	-99,955	-100,103	-100,758	-99,724	-101,259
	2,0 - 3,0	-99,273	-105,752	-102,950	-104,180	-103,732	-104,225
	3,0 - 4,0	-97,915	-107,702	-105,553	-107,306	-104,378	-107,682
	4,0 - 5,0	-101,820	-110,562	-108,908	-109,817	-110,086	-110,414

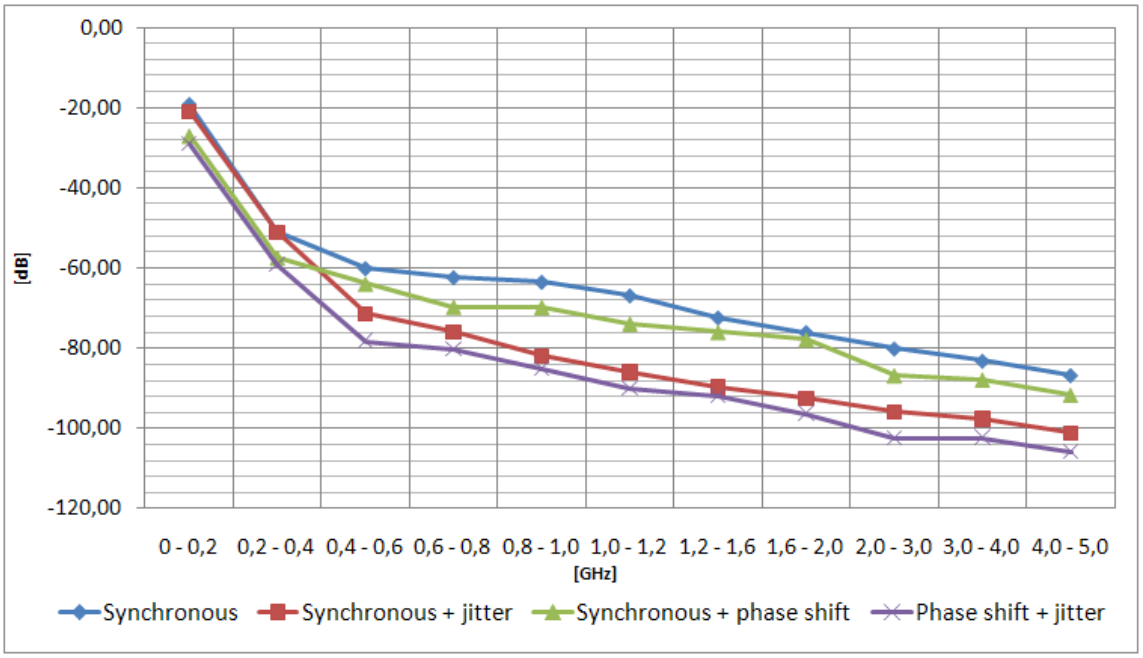

Figure 4.1. EMI characteristic in the 4-module synchronous systems

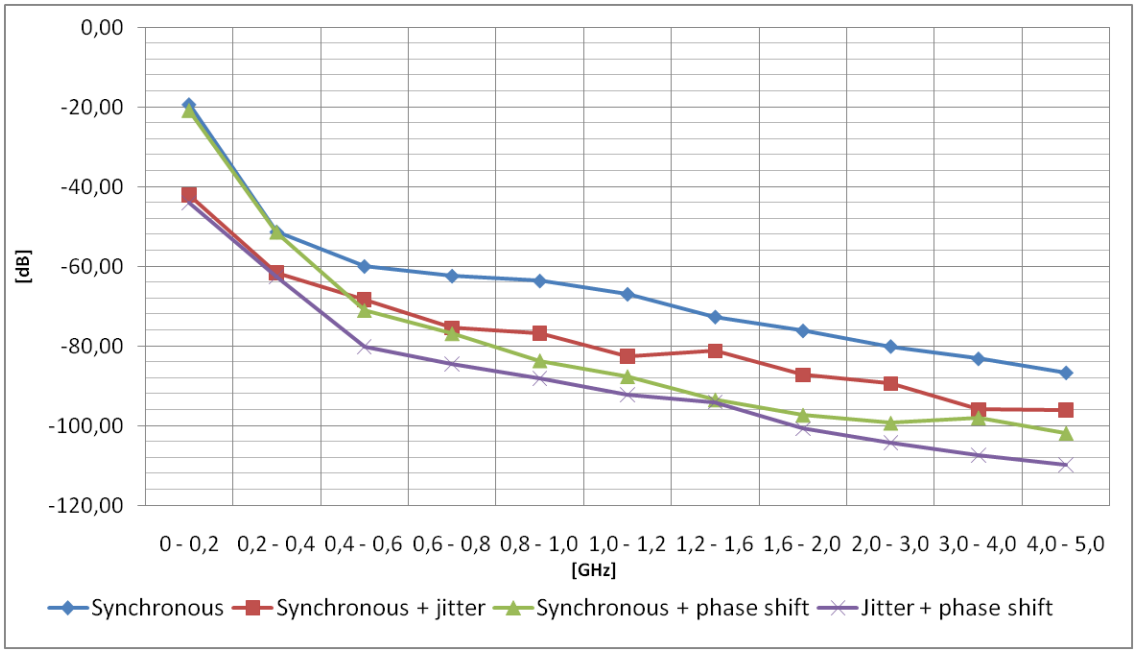

Figure 4.2. EMI characteristic in the 10-module synchronous systems

In Figures 4.1 and 4.2, it can be observed the aggregated EMI characteristic and its reduction in 4-module and 10-module synchronous systems respectively. In particular, it can be seen the EMI reduction in the synchronous system with a jitter applied. As it is noticeable, the jitter reduces only higher frequencies starting from 400 MHz. It has no significant influence on the lower spectral range. However, to achieve the reduction, the circuit should be immune to 10% jitter, which is not so easy in a synchronous design, both for hold and setup time optimization. Moreover, Figures 4.1 and 4.2 show the effects of adding a phase shift to a system. Cases with 0%, 10%, 20%, 30% and 0%, 50%, 20%, 40%, 70%, 90%, 10%, 30%, 60%, and 80% phase shift of a clock period have been modeled.[1]

By introducing a phase shift to a circuit, EMI in a low frequency range can be alleviated, thus reducing current peaks. The high frequency spectrum remains not significantly changed compared to a basic synchronous approach. The tests were conducted also with a combination of jitter and phase shift. The results are very promising because they incorporate advantages of the both features. However, it would be a real challenge to guarantee safe data transfer between blocks in such synchronous system.

[1] In practice, implementation of such a synchronous system is unfeasible and these results should be treated as extremely unattainable for practical systems.

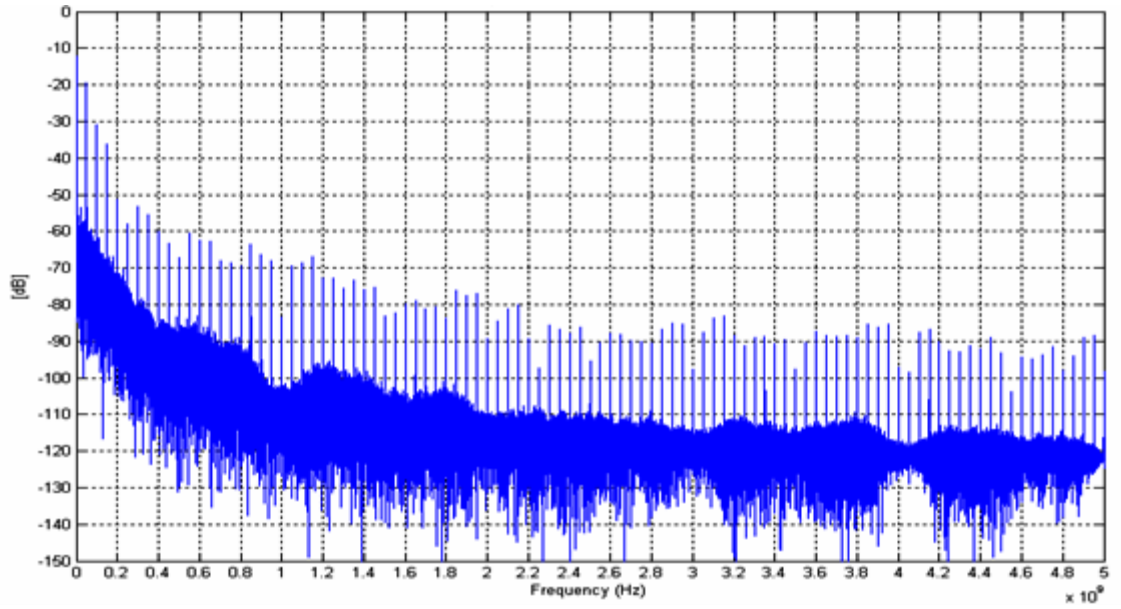

Figure 4.3 Single-sided power spectrum of supply current for the 10-module totally synchronous circuit

The impact of a system granularity on EMI reduction can be observed by comparing Figures 4.1 and 4.2. Adding a phase shift in the 10-module design improves EMI reduction more than in the 4-module one. However, in a less granular approach the influence of jitter is more visible. Furthermore, the overall reduction with jitter and phase shift added to a system is approximately 5 dB higher in a more granular design. Hence, it can be concluded that the more granular design, the better EMI reduction. It is also more reasonable approach, because added phase shift alone reduces EMI significantly. Adding a phase shift to a system is more feasible than combination of phase shift and jitter. Combining those two features would require a hard to design timing constraints in a chip.

In Figures 4.3 and 4.4 the single-sided amplitude spectrums are presented. The former figure presents a spectrum of totally synchronous 10-module design. The latter one presents the same system with the phase shift and the jitter feature applied. A significant lowering of the envelope can be observed. Additionally, the peaks in a system with phase shift and jitter are almost totally prevented and there are only few in a low range of frequencies. In order to alleviate them, it would be necessary to reduce current peaks in a system, which is not a trivial task.

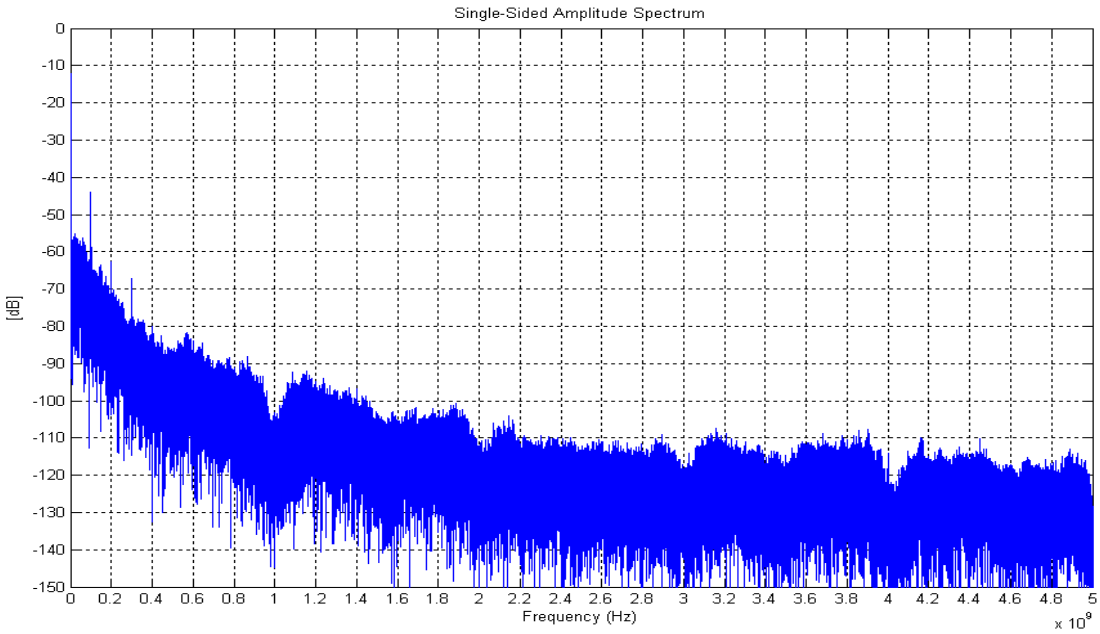

Figure 4.4. Power spectrum of supply current for the 10-module synchronous circuit with added jitter and phase shifts distributed: 0%, 50%, 20%, 40%, 70%, 90%, 10%, 30%, 60%, and 80%

4.2. Evaluating GALS systems

Simulation results for GALS 4-module and 10-module systems with different features are presented in detail in Tables 4.4, 4.5, 4.6, 4.7, 4.8, 4.9 and 4.10. As mentioned before, GALS systems have been modeled with different granularities, sets of frequencies, topologies, and clock jitters. The results are presented in dB, in 11 ranges. The aim of testing the GALS approach was to investigate the possibility of EMI reduction in asynchronous designs with comparison to synchronous designs. At the first glance it is noticeable, the major differences in EMI reduction with different parameters. There is high correlation between reduction of EMI and the features settings.

Simulation results of a mesh topology are limited because of the lack of exact clock behavior. It was caused by the handshake jams with several frequency sets and data transfer scenarios. The handshake jams were the main reason for the problem occurring is a system's topology, where each block is connected to all others. It leads to an inappropriate fulfilling handshake timing constrains and deadlock. It crashes the whole system by stopping one of the local clock generators in a low state for the rest of a simulation. This however goes beyond the scope of this thesis; hence, it will not be investigated in details.

Table 4.4 Simulation results for the 4-module GALS point-to-point topology system without clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter

Simulation type		A1	A2	A3	B1	B2	B3	C1	C2	C3
Parameters	Modules' frequencies [MHz]	49,50	45,45	100,00	49,50	45,45	100,00	49,50	45,45	100,00
		51,02	62,50	50,00	51,02	62,50	50,00	51,02	62,50	50,00
		50,00	50,00	33,33	50,00	50,00	33,33	50,00	50,00	33,33
		49,02	41,67	50,00	49,02	41,67	50,00	49,02	41,67	50,00
	Jitter	no	no	no	no	no	no	no	no	no
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-17,53	-25,77	-21,46	-18,47	-27,55	-25,28	-18,86	-26,52	-27,57
	0,2 - 0,4	-60,48	-60,43	-45,58	-58,90	-57,42	-51,68	-59,39	-58,69	-55,56
	0,4 - 0,6	-67,70	-61,42	-61,10	-68,91	-62,50	-61,82	-67,77	-61,70	-62,65
	0,6 - 0,8	-67,65	-67,52	-70,58	-71,38	-70,53	-70,06	-71,33	-70,10	-67,93
	0,8 - 1,0	-71,79	-70,50	-69,70	-71,30	-69,62	-71,36	-70,83	-71,94	-75,86
	1,0 - 1,2	-75,06	-72,26	-72,45	-75,17	-72,26	-73,31	-77,26	-70,57	-77,70
	1,2 - 1,6	-80,78	-74,22	-74,97	-80,01	-75,37	-75,87	-81,18	-78,86	-77,70
	1,6 - 2,0	-84,23	-82,96	-78,73	-85,03	-81,55	-80,39	-85,15	-79,95	-80,64
	2,0 - 3,0	-87,72	-84,23	-82,35	-87,16	-85,45	-84,70	-88,39	-84,32	-89,80
	3,0 - 4,0	-89,92	-88,35	-85,03	-89,74	-88,67	-88,58	-91,67	-87,71	-88,60
	4,0 - 5,0	-92,56	-91,88	-86,65	-93,64	-89,27	-89,79	-94,36	-92,20	-90,47

Table 4.5. Simulation results for the 4-module GALS point-to-point topology system with clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter

Simulation type		A1	A2	A3	B1	B2	B3	C1	C2	C3
Parameters	Modules' frequencies [MHz]	49,50	45,45	100,00	49,50	45,45	100,00	49,50	45,45	100,00
		51,02	62,50	50,00	51,02	62,50	50,00	51,02	62,50	50,00
		50,00	50,00	33,33	50,00	50,00	33,33	50,00	50,00	33,33
		49,02	41,67	50,00	49,02	41,67	50,00	49,02	41,67	50,00
	Jitter	yes	yes	yes	yes	yes	yes	yes	yes	yes
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-17,92	-25,29	-22,35	-19,42	-27,72	-26,30	-19,76	-27,24	-28,12
	0,2 - 0,4	-61,15	-64,35	-45,86	-60,98	-56,91	-52,83	-63,04	-58,18	-56,58
	0,4 - 0,6	-79,40	-72,58	-68,25	-78,49	-71,96	-69,55	-77,72	-72,15	-72,28
	0,6 - 0,8	-79,84	-81,19	-75,53	-81,02	-82,48	-77,12	-81,20	-81,87	-78,58
	0,8 - 1,0	-84,45	-85,96	-81,25	-85,43	-83,35	-82,97	-86,72	-85,54	-87,33
	1,0 - 1,2	-89,28	-89,06	-88,13	-89,08	-89,34	-88,63	-88,19	-87,81	-90,45
	1,2 - 1,6	-90,15	-91,80	-91,13	-90,32	-92,38	-89,78	-90,39	-91,09	-90,85
	1,6 - 2,0	-96,07	-96,61	-96,78	-98,18	-96,63	-95,68	-98,78	-96,62	-97,75
	2,0 - 3,0	-103,03	-100,85	-101,91	-102,89	-99,95	-100,39	-102,93	-100,83	-103,19
	3,0 - 4,0	-104,85	-105,74	-104,94	-105,99	-102,70	-102,65	-105,50	-104,65	-105,03
	4,0 - 5,0	-106,21	-108,10	-105,24	-108,88	-108,63	-105,17	-108,85	-107,72	-107,69

Table 4.6. Simulation results for the 4-module GALS star topology system without clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter

Simulation type		A1	A2	A3	B1	B2	B3	C1	C2	C3
Parameters	Modules' frequencies [MHz]	49,50	45,45	100,00	49,50	45,45	100,00	49,50	45,45	100,00
		51,02	62,50	50,00	51,02	62,50	50,00	51,02	62,50	50,00
		50,00	50,00	33,33	50,00	50,00	33,33	50,00	50,00	33,33
		49,02	41,67	50,00	49,02	41,67	50,00	49,02	41,67	50,00
	Jitter	no	no	no	no	no	no	no	no	no
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-29,594	-31,436	-21,429	-28,166	-28,482	-21,408	-28,512	-26,089	-21,552
	0,2 - 0,4	-56,463	-57,989	-45,662	-62,223	-57,368	-45,071	-64,846	-53,779	-48,274
	0,4 - 0,6	-69,641	-64,104	-61,000	-67,984	-65,123	-60,967	-65,671	-65,850	-61,196
	0,6 - 0,8	-74,062	-69,078	-64,816	-72,390	-72,640	-64,657	-74,371	-69,390	-67,272
	0,8 - 1,0	-73,987	-68,310	-69,363	-74,164	-75,438	-69,595	-74,597	-76,344	-69,639
	1,0 - 1,2	-77,992	-74,516	-70,127	-73,479	-75,438	-70,189	-73,825	-72,954	-69,810
	1,2 - 1,6	-80,848	-76,297	-74,870	-80,975	-80,271	-75,303	-80,472	-80,437	-75,124
	1,6 - 2,0	-84,453	-85,182	-79,153	-86,205	-87,235	-79,399	-81,098	-87,603	-79,660
	2,0 - 3,0	-90,791	-83,953	-83,445	-89,896	-85,495	-83,350	-88,347	-84,090	-83,303
	3,0 - 4,0	-87,988	-91,433	-85,870	-89,981	-92,228	-85,967	-89,401	-92,291	-86,060
	4,0 - 5,0	-95,431	-90,652	-88,693	-94,915	-91,612	-88,834	-94,072	-92,653	-89,001

Table 4.7. Simulation results for the 4-module GALS star topology system with clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter

Simulation type		A1	A2	A3	B1	B2	B3	C1	C2	C3
Parameters	Modules' frequencies [MHz]	49,50	45,45	100,00	49,50	45,45	100,00	49,50	45,45	100,00
		51,02	62,50	50,00	51,02	62,50	50,00	51,02	62,50	50,00
		50,00	50,00	33,33	50,00	50,00	33,33	50,00	50,00	33,33
		49,02	41,67	50,00	49,02	41,67	50,00	49,02	41,67	50,00
	Jitter	yes	yes	yes	yes	yes	yes	yes	yes	yes
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-29,819	-31,263	-22,401	-29,582	-28,314	-22,445	-29,259	-25,824	-22,537
	0,2 - 0,4	-58,908	-62,834	-46,463	-66,001	-60,176	-46,930	-63,019	-55,391	-46,327
	0,4 - 0,6	-78,294	-73,901	-68,077	-79,170	-74,171	-68,709	-77,566	-77,183	-67,540
	0,6 - 0,8	-82,108	-82,058	-75,346	-81,696	-82,659	-75,798	-81,821	-82,742	-76,636
	0,8 - 1,0	-87,151	-82,684	-80,228	-84,713	-86,894	-82,193	-86,504	-85,745	-81,737
	1,0 - 1,2	-88,086	-89,592	-88,126	-87,230	-89,080	-87,790	-88,260	-88,407	-89,100
	1,2 - 1,6	-90,875	-91,505	-88,981	-92,096	-92,257	-89,914	-91,365	-93,563	-90,791
	1,6 - 2,0	-96,363	-95,866	-95,681	-98,094	-97,416	-94,235	-96,129	-97,631	-96,085
	2,0 - 3,0	-103,206	-100,060	-98,603	-103,679	-101,748	-100,863	-103,909	-102,268	-98,503
	3,0 - 4,0	-102,074	-105,492	-104,125	-105,230	-105,225	-104,347	-104,956	-106,565	-104,455
	4,0 - 5,0	-105,408	-107,423	-106,061	-106,862	-107,005	-106,578	-107,506	-109,483	-106,464

Table 4.8. Simulation results for the 10-module GALS star topology system without clock jitter, with different sets of frequencies (1, 2, 3, 4, 5) and various data transfer scenarios (A, B, C) described in details in the previous chapter

Simulation type		A1	A2	A3	A4	A5	B1	B2	B3	B4	B5	C1	C2	C3	C4	C5
Parameters	Modules' frequencies [MHz]	49,02	41,67	83,33	71,43	71,43	49,02	41,67	83,33	71,43	71,43	49,02	41,67	83,33	71,43	71,43
		48,08	35,71	90,91	55,56	55,56	48,08	35,71	90,91	55,56	55,56	48,08	35,71	90,91	55,56	55,56
		47,17	55,56	100,00	35,71	35,71	47,17	55,56	100,00	35,71	35,71	47,17	55,56	100,00	35,71	35,71
		51,02	71,43	31,25	41,67	41,67	51,02	71,43	31,25	41,67	41,67	51,02	71,43	31,25	41,67	41,67
		52,08	33,33	33,33	33,33	83,33	52,08	33,33	33,33	33,33	83,33	52,08	33,33	33,33	33,33	83,33
		53,19	45,45	100,00	62,50	62,50	53,19	45,45	100,00	62,50	62,50	53,19	45,45	100,00	62,50	62,50
		49,02	38,46	83,33	38,46	38,46	49,02	38,46	83,33	38,46	38,46	49,02	38,46	83,33	38,46	38,46
		47,17	62,50	33,33	45,45	45,45	47,17	62,50	33,33	45,45	45,45	47,17	62,50	33,33	45,45	45,45
		46,30	83,33	35,71	50,00	50,00	46,30	83,33	35,71	50,00	50,00	46,30	83,33	35,71	50,00	50,00
		50,00	50,00	50,00	83,33	33,33	50,00	50,00	50,00	83,33	33,33	50,00	50,00	50,00	83,33	33,33
	Jitter	no	no	no	no	no	no	no	no	no	no	no	no	no	no	no
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-29,556	-30,931	-32,945	-32,760	-32,420	-30,048	-30,143	-33,013	-31,674	-32,737	-30,743	-29,694	-32,927	-31,999	-32,581
	0,2 - 0,4	-62,564	-55,355	-45,860	-50,392	-50,276	-63,305	-55,599	-47,563	-50,254	-50,696	-62,926	-54,773	-45,423	-50,869	-50,554
	0,4 - 0,6	-72,809	-66,036	-63,839	-62,347	-62,871	-72,795	-65,762	-64,028	-61,996	-62,872	-73,411	-65,202	-63,350	-62,487	-62,614
	0,6 - 0,8	-73,167	-72,544	-67,354	-69,087	-69,118	-72,210	-71,882	-67,355	-69,060	-69,460	-71,618	-71,462	-66,787	-68,455	-69,683
	0,8 - 1,0	-76,415	-75,655	-66,085	-73,070	-72,940	-75,966	-75,527	-66,703	-73,118	-73,157	-76,280	-76,162	-66,715	-72,715	-74,020
	1,0 - 1,2	-77,516	-75,655	-66,085	-76,444	-73,425	-77,747	-75,527	-66,703	-76,650	-73,157	-77,725	-76,162	-66,715	-76,633	-74,020
	1,2 - 1,6	-87,182	-82,570	-76,626	-76,486	-76,252	-86,614	-82,219	-76,255	-76,318	-76,769	-86,954	-82,285	-76,190	-76,584	-76,652
	1,6 - 2,0	-88,319	-86,371	-77,995	-80,877	-81,092	-89,387	-85,816	-77,774	-80,938	-81,317	-87,848	-86,111	-77,655	-81,024	-81,555
	2,0 - 3,0	-93,500	-88,188	-77,758	-85,439	-85,537	-93,523	-88,042	-77,775	-85,699	-85,810	-93,147	-88,448	-77,865	-86,185	-86,669
	3,0 - 4,0	-96,790	-91,744	-86,225	-89,659	-89,356	-96,872	-91,951	-86,880	-89,859	-89,563	-96,539	-92,190	-86,458	-90,254	-90,223
	4,0 - 5,0	-98,518	-94,419	-86,649	-89,195	-89,121	-98,136	-94,037	-86,706	-89,813	-89,893	-97,489	-94,400	-86,102	-89,514	-90,148

Table 4.9. Simulation results for the 10-module GALS star topology system with clock jitter, with different sets of frequencies (1, 2, 3, 4, 5) and various data transfer scenarios (A, B, C) described in details in the previous chapter

Simulation type		A1	A2	A3	A4	A5	B1	B2	B3	B4	B5	C1	C2	C3	C4	C5
Parameters	Modules' frequencies [MHz]	49,02	41,67	83,33	71,43	71,43	49,02	41,67	83,33	71,43	71,43	49,02	41,67	83,33	71,43	71,43
		48,08	35,71	90,91	55,56	55,56	48,08	35,71	90,91	55,56	55,56	48,08	35,71	90,91	55,56	55,56
		47,17	55,56	100,00	35,71	35,71	47,17	55,56	100,00	35,71	35,71	47,17	55,56	100,00	35,71	35,71
		51,02	71,43	31,25	41,67	41,67	51,02	71,43	31,25	41,67	41,67	51,02	71,43	31,25	41,67	41,67
		52,08	33,33	33,33	33,33	83,33	52,08	33,33	33,33	33,33	83,33	52,08	33,33	33,33	33,33	83,33
		53,19	45,45	100,00	62,50	62,50	53,19	45,45	100,00	62,50	62,50	53,19	45,45	100,00	62,50	62,50
		49,02	38,46	83,33	38,46	38,46	49,02	38,46	83,33	38,46	38,46	49,02	38,46	83,33	38,46	38,46
		47,17	62,50	33,33	45,45	45,45	47,17	62,50	33,33	45,45	45,45	47,17	62,50	33,33	45,45	45,45
		46,30	83,33	35,71	50,00	50,00	46,30	83,33	35,71	50,00	50,00	46,30	83,33	35,71	50,00	50,00
		50,00	50,00	50,00	83,33	33,33	50,00	50,00	50,00	83,33	33,33	50,00	50,00	50,00	83,33	33,33
	Jitter	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-30,000	-30,984	-32,160	-32,400	-32,345	-30,380	-30,278	-32,072	-31,390	-32,245	-31,607	-29,902	-32,111	-32,004	-32,189
	0,2 - 0,4	-68,956	-59,729	-46,154	-49,702	-49,363	-68,345	-54,436	-48,332	-50,083	-49,780	-59,604	-54,725	-45,587	-50,207	-49,815
	0,4 - 0,6	-82,658	-80,047	-69,768	-74,202	-73,136	-82,721	-78,883	-70,389	-72,136	-73,299	-77,562	-76,981	-70,975	-73,339	-73,337
	0,6 - 0,8	-85,217	-86,858	-73,611	-85,318	-84,513	-84,784	-87,084	-75,182	-84,896	-83,760	-84,173	-87,449	-75,865	-84,778	-84,054
	0,8 - 1,0	-89,325	-90,534	-84,787	-87,433	-87,507	-89,398	-89,856	-84,857	-86,552	-86,035	-90,507	-90,954	-85,534	-86,059	-86,742
	1,0 - 1,2	-91,972	-93,003	-84,787	-90,154	-90,522	-92,732	-94,105	-84,857	-90,799	-91,647	-93,179	-92,761	-85,534	-92,550	-90,770
	1,2 - 1,6	-94,876	-97,453	-89,225	-92,489	-93,690	-94,890	-97,262	-87,828	-92,536	-91,216	-96,426	-95,042	-89,146	-92,193	-93,855
	1,6 - 2,0	-101,469	-98,943	-96,211	-96,799	-96,085	-101,352	-99,794	-96,629	-95,680	-95,765	-100,524	-100,378	-95,163	-96,463	-94,641
	2,0 - 3,0	-107,454	-103,642	-96,212	-101,799	-101,067	-106,930	-104,477	-97,083	-102,359	-100,635	-103,910	-104,527	-96,418	-101,635	-101,725
	3,0 - 4,0	-109,770	-107,176	-104,178	-106,972	-106,864	-109,432	-109,979	-102,664	-107,972	-106,285	-108,440	-108,621	-103,749	-107,684	-106,917
	4,0 - 5,0	-111,127	-108,779	-104,017	-108,500	-108,189	-111,871	-111,262	-104,330	-108,171	-107,921	-110,344	-111,120	-106,482	-108,591	-107,743

Table 4.10. Simulation results for the 4-module GALS mesh topology system with and without clock jitter, with different sets of frequencies (1, 2, 3) and various data transfer scenarios (A, B, C) described in details in the previous chapter

Simulation type		A1	A3	B1	A1	A3	B1
Parameters	Modules' frequencies [MHz]	49,50	100,00	49,50	49,50	100,00	49,50
		51,02	50,00	51,02	51,02	50,00	51,02
		50,00	33,33	50,00	50,00	33,33	50,00
		49,02	50,00	49,02	49,02	50,00	49,02
	Jitter	No	No	No	Yes	Yes	Yes
Results [dB] at 11 frequency ranges [GHz]	0 - 0,2	-22,549	-31,153	-31,065	-23,100	-31,560	-32,871
	0,2 - 0,4	-62,128	-57,696	-61,142	-63,955	-61,369	-65,947
	0,4 - 0,6	-66,104	-61,660	-67,406	-78,733	-68,726	-78,082
	0,6 - 0,8	-68,687	-76,876	-69,748	-81,142	-81,489	-80,773
	0,8 - 1,0	-73,144	-74,394	-72,414	-86,687	-87,911	-87,991
	1,0 - 1,2	-74,170	-76,292	-77,263	-88,148	-89,529	-89,284
	1,2 - 1,6	-81,088	-76,292	-82,348	-90,837	-89,657	-91,013
	1,6 - 2,0	-84,847	-80,164	-85,353	-97,867	-97,965	-98,955
	2,0 - 3,0	-88,271	-83,279	-88,073	-102,841	-100,620	-102,852
	3,0 - 4,0	-89,759	-88,640	-92,691	-104,642	-103,720	-105,548
	4,0 - 5,0	-92,726	-89,946	-94,149	-106,855	-107,371	-109,490

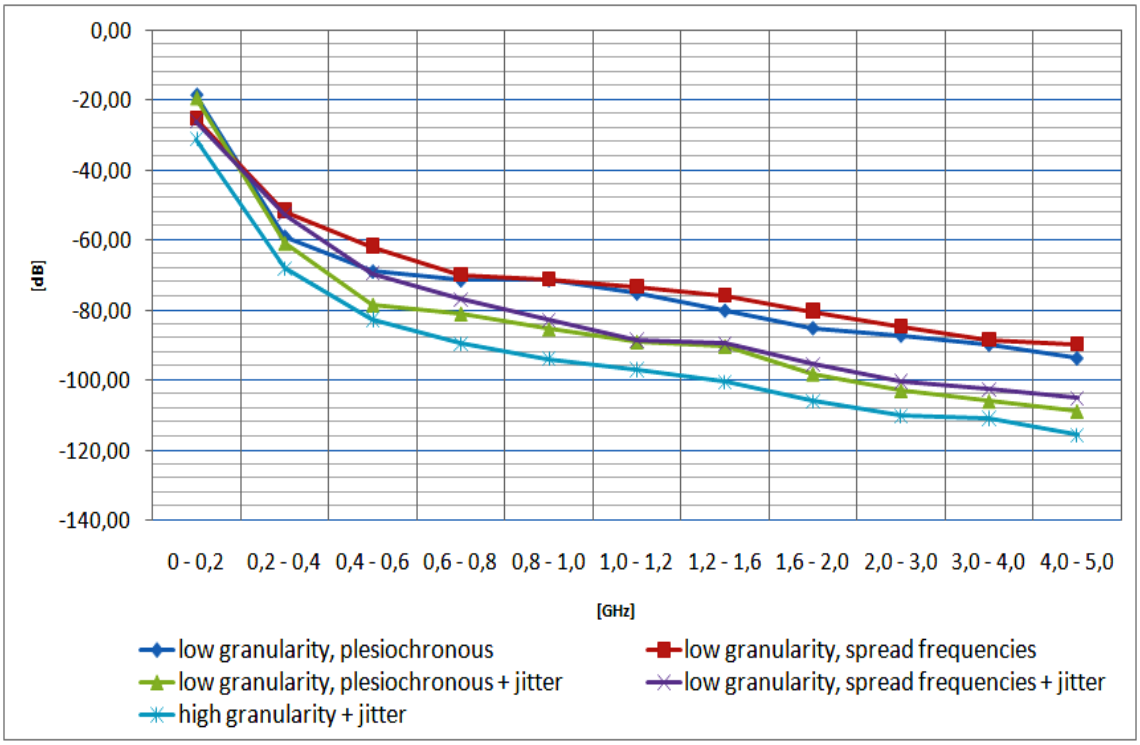

Figure 4.5. EMI characteristic in GALS systems with different frequencies set and jitter

Figure 4.5 represents the results of comparing two sets of frequencies with medium data transfer and also shows the behavior for low granularity systems (4 GALS blocks) and high granularity systems (10 GALS blocks). It can be observed that plesiochronous systems can achieve a significant EMI reduction in a high frequency range. However, it does not improve EMI for low frequency operation. On the other hand, the GALS system with a larger difference of frequencies reduces EMI much better in a spectrum of low frequencies, still preserving good parameters for higher frequencies. The test performed on various transfers rate with the same frequency has shown very little difference in EMI reduction. The range of the result variations did not exceed 5 dB.

Figure 4.5 shows the EMI reduction in GALS systems with added jitter. It can be observed that there is almost no impact from the jitter at low frequencies. It remains almost the same as in GALS systems without jitter. However, the higher frequency range is more attenuated giving a better reduction of EMI. Every set of frequencies has a similar spectrum starting from 400 MHz and reductions around 15 dB can be observed.

Comparing 3 structures of 4-modules GALS systems: point-to-point, mesh and star, a similar behavior was noticed. There is a very little influence of data rate transfer intensity on EMI reduction. The most important parameter is the frequency of LS blocks. The more frequency spread, the higher EMI reduction in the lower spectrum. Moreover, in each case the jitter has a positive effect on the reduction of EMI. It significantly reduces higher frequencies in a spectrum. The average reduction of EMI for all 4-module topologies in comparison to the totally synchronous system is around 20 dB starting from 400 MHz.

Similar results can be extracted from the star topology with more satellite blocks. However, greater difference in EMI reduction is noticeable after adding jitter. The frequency sets where the centre clock is the slowest one present worst result. From the perspective of EMI better results are achieved when the center block is the fastest one. Hence, it can be concluded that the most reasonable architecture from the point of view of the performance, with the fastest center block, is also the most appropriate approach for the EMI reduction.

The effect of block granularity was also compared to the final results. Comparing 4-module and 10-module GALS system, it can be observed the better results for a more granular design; this can be clearly observed in Figure 4.5. The gain reduction is around 5 dB. In general, it means that the finer the granularity of the system, the better reduction of EMI.

4.2.1. GALS granularity vs EMI reduction limits

In the previous section it was shown in the simulations that GALS granularity has a significant effect on EMI profile. However, it is very important to investigate this effect and to observe to what extent it is possible to reduce the EMI by deeper GALS partitioning of the system [27]. In order to perform this task a series of simulations based on the same starting system has been completed. Since GALS-ification could have many different parameters (granularity, frequency setup of the local blocks, jitter effects, topology of the resulting system, etc.), the following analysis have been done. The starting point was a pure synchronous system without any sub-blocks. The basic frequency was defined for this system (as in the previous simulations - 50 MHz) and basic current profiles. Afterwards GALS partitioning was introduced and the number of GALS blocks increased, but the same total energy of the system was kept. The partitioned blocks are modeled such that they have plesiochronous behavior around the same median synchronous frequency. All settings are presented in tables 4.11, 4.12, 4.13, 4.14.

Table 4.11. Frequencies distribution for different partitioning of GALS model

Number of blocks	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Frequencies [MHz]																				
1	50	48	48	48	48	47	47	47	47	47	47	47	47	47	47	47	47	47	47	47
2		52	50	49	49	48	48	48	48	48	48	48	47,5	47,5	47,5	47,5	47,5	47,5	47,5	47,5
3			52	51	50	49	49	49	49	49	48,5	48,5	48	48	48	48	48	48	48	48
4				52	51	51	50	49,5	49,5	49,5	49	49	48,5	48,5	48,5	48,5	48,5	48,5	48,5	48,25
5					52	52	51	50	50	50	49,5	49,5	49	49	49	49	49	48,75	48,75	48,5
6						53	52	51	50,5	50,5	50	50	49,5	49,5	49,5	49,25	49,25	49	49	48,75
7							53	52	51	51	50,5	50,5	50	50	49,75	49,5	49,5	49,25	49,25	49
8								53	52	51,5	51	51	50,5	50,25	50	49,75	49,75	49,5	49,5	49,25
9									53	52	51,5	51,5	51	50,5	50,25	50	50	49,75	49,75	49,5
10										53	52	52	51,5	51	50,5	50,25	50,25	50	50	49,75
11											53	52,5	52	51,5	51	50,5	50,5	50,25	50,25	50
12												53	52,5	52	51,5	51	50,75	50,5	50,5	50,25
13													53	52,5	52	51,5	51	50,75	50,75	50,5
14														53	52,5	52	51,5	51	51	50,75
15															53	52,5	52	51,5	51,25	51
16																53	52,5	52	51,5	51,25
17																	53	52,5	52	51,5
18																		53	52,5	52
19																			53	52,5
20																				53
Average	50,00	50,00	50,00	50,00	50,00	50,00	50,00	49,94	50,00	50,15	50,00	50,21	50,00	50,02	50,00	49,95	50,00	49,93	50,00	49,91

Table 4.12. Maximal current distribution per GALS module for different partitioning of GALS model

Current peaks [mA]	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	1000	500	333	250	200	166	143	125	111	100	91	84	77	72	67	62,5	58	56	53	50
2		500	333	250	200	166	143	125	111	100	91	84	77	72	67	62,5	58	55,5	53	50
3			334	250	200	166	143	125	111	100	91	83	77	72	67	62,5	59	55,5	53	50
4				250	200	166	143	125	111	100	91	83	77	71	67	62,5	59	55,5	53	50
5					200	166	143	125	111	100	91	83	77	71	67	62,5	59	55,5	53	50
6						170	143	125	111	100	91	83	77	71	66	62,5	59	55,5	53	50
7							142	125	111	100	91	83	77	71	66	62,5	59	55,5	52	50
8								125	111	100	91	83	77	71	66	62,5	59	55,5	52	50
9									112	100	91	83	77	71	66	62,5	59	55,5	52	50
10										100	91	83	77	71	66	62,5	59	55,5	52	50
11											90	84	77	71	67	62,5	59	55,5	52	50
12												84	77	72	67	62,5	59	55,5	52	50
13													76	72	67	62,5	59	55,5	52	50
14														72	67	62,5	59	55,5	53	50
15															67	62,5	59	55,5	53	50
16																62,5	59	55,5	53	50
17																	58	55,5	53	50
18																		56	53	50
19																			53	50
20																				50
Sum	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000

Table 4.13. Initial phase shift distribution among GALS modules for different partitioning of GALS model

Phase shift [%]	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2		50	33	25	20	15	10	10	10	10	5	5	5	5	5	5	5	5	5	5
3			66	50	40	30	20	20	20	20	10	10	10	10	10	10	10	10	10	10
4				75	60	45	30	30	30	30	20	15	15	15	15	15	15	15	15	15
5					80	60	40	40	40	40	30	20	20	20	20	20	20	20	20	20
6						75	50	50	50	50	40	30	25	25	25	25	25	25	25	25
7							60	60	60	60	50	40	30	30	30	30	30	30	30	30
8								70	70	70	60	50	40	35	35	35	35	35	35	35
9									80	80	70	60	50	40	40	40	40	40	40	40
10										90	80	70	60	50	45	45	45	45	45	45
11											90	80	70	60	50	50	50	50	50	50
12												90	80	70	60	55	55	55	55	55
13													90	80	70	60	60	60	60	60
14														90	80	70	65	65	65	65
15															90	80	70	70	70	70
16																90	80	75	75	75
17																	90	80	80	80
18																		90	85	85
19																			90	90
20																				95

Table 4.14. Results of EMI reduction with GALS system partitioning ranging from 1 module up to 20 modules

Results [GHz]/[dB]	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0 - 0,2	-25,9109	-34,1154	-36,2381	-37,2323	-38,7851	-40,5949	-42,516	-43,0774	-43,9312	-44,9671	-45,3731	-46,2691	-47,1702	-47,303	-48,4492	-48,7295	-49,7553	-49,8416	-50,9026	-50,9496
0,2 - 0,4	-38,6534	-44,398	-45,9012	-50,1504	-50,4137	-51,9987	-53,0662	-54,3773	-55,2817	-56,3841	-57,1811	-57,9028	-58,5641	-59,2227	-60,2748	-60,6976	-61,1398	-62,4321	-61,7801	-62,5447
0,4 - 0,6	-56,3118	-61,7084	-61,1401	-67,6728	-67,938	-67,6473	-68,0792	-71,8839	-70,6421	-71,0167	-71,4129	-72,0936	-73,7241	-73,4836	-74,6015	-75,5926	-76,859	-76,0538	-77,8778	-76,8311
0,6 - 0,8	-56,2446	-62,0967	-65,0223	-67,4974	-67,3661	-69,0026	-72,2651	-72,1333	-71,1297	-73,3963	-74,0576	-73,474	-75,1262	-75,7	-76,1924	-77,2378	-78,3222	-79,0212	-77,2415	-78,997
0,8 - 1,0	-59,0993	-65,3375	-67,6009	-71,0982	-70,7699	-72,5107	-74,7426	-75,1729	-76,422	-77,0015	-78,0421	-80,2031	-80,8476	-81,429	-82,4092	-82,0106	-82,099	-82,1207	-81,7592	-81,9155
1,0 - 1,2	-67,6312	-71,7593	-74,9973	-77,6554	-79,4737	-80,5307	-82,2058	-83,4799	-84,136	-84,3675	-85,6862	-86,6657	-86,573	-87,9501	-87,9818	-88,3991	-86,6676	-88,0437	-84,2287	-85,4221
1,2 - 1,6	-65,3512	-72,2282	-74,0779	-78,2737	-77,6468	-80,6381	-80,6125	-83,4654	-83,0809	-84,5501	-85,6276	-86,4687	-86,0364	-86,4894	-88,3607	-86,989	-88,0781	-90,3323	-90,0865	-89,1403
1,6 - 2,0	-72,5812	-77,7228	-80,9821	-82,7633	-83,9238	-85,5321	-87,3528	-88,3788	-88,2491	-89,7968	-90,4042	-90,8211	-92,1423	-92,1437	-93,2304	-92,5317	-92,5038	-94,7429	-94,708	-95,3787
2,0 - 3,0	-75,3294	-81,2845	-82,9879	-87,1369	-87,2328	-89,3486	-90,0246	-91,8209	-93,4779	-93,8492	-94,4562	-92,8144	-94,5792	-95,3994	-95,5182	-96,5981	-98,6474	-96,9378	-96,3727	-98,1443
3,0 - 4,0	-81,3188	-86,0361	-87,6677	-89,5839	-91,1815	-93,041	-93,3735	-96,2703	-96,8625	-97,2574	-98,2827	-99,5874	-96,6058	-96,8834	-97,5392	-98,41	-98,6877	-99,3836	-99,016	-97,3944
4,0 - 5,0	-82,5241	-87,0817	-88,8523	-91,5971	-93,1327	-94,9992	-96,3343	-97,9327	-99,3272	-99,844	-100,779	-101,136	-102,238	-102,341	-102,899	-103,613	-104,498	-105,22	-104,111	-104,487
Sum	-680,9559	-743,7686	-765,4678	-800,6614	-807,8641	-825,8439	-840,5726	-857,9928	-862,5403	-872,4307	-881,3027	-887,4359	-893,6069	-898,3453	-907,4564	-910,809	-917,2579	-924,1297	-918,0841	-921,2047

The results of those simulations are given in Figures 4.6, 4.7 and 4.8. The figures show the dependency of EMI in different frequency ranges for different GALS granularity. In Figure 4.6 and 4.7 it can been noticed how granularity affects the EMI reduction.

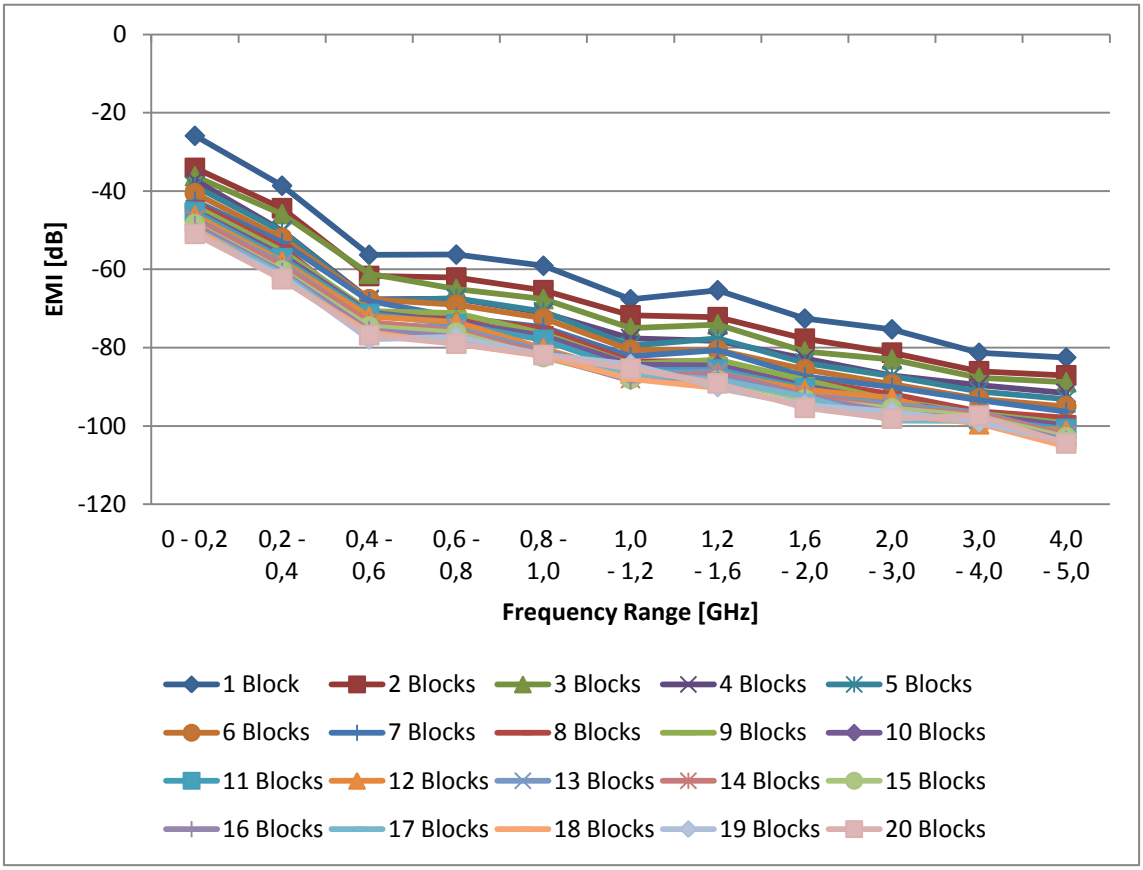

Figure 4.6. Reduction of EMI for different GALS granularity

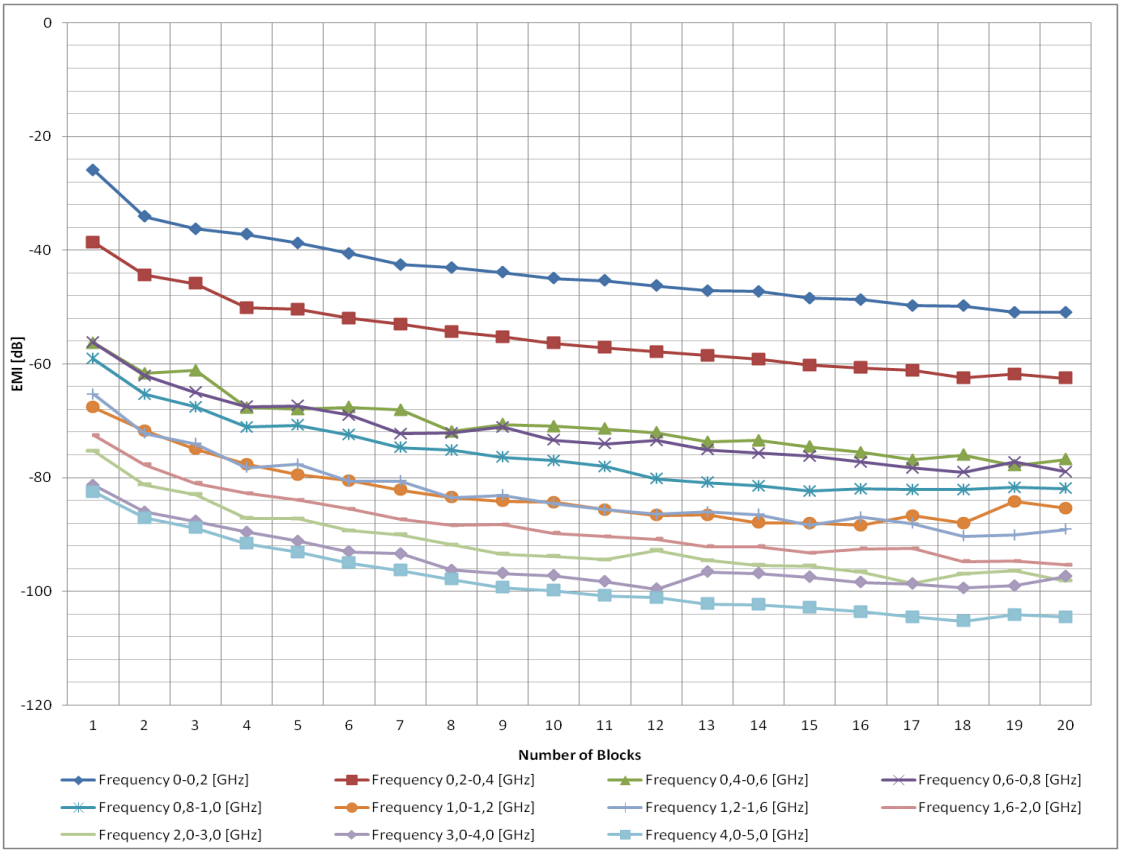

Figure 4.7. Reduction of EMI with different GALS granularity among different ranges of frequencies

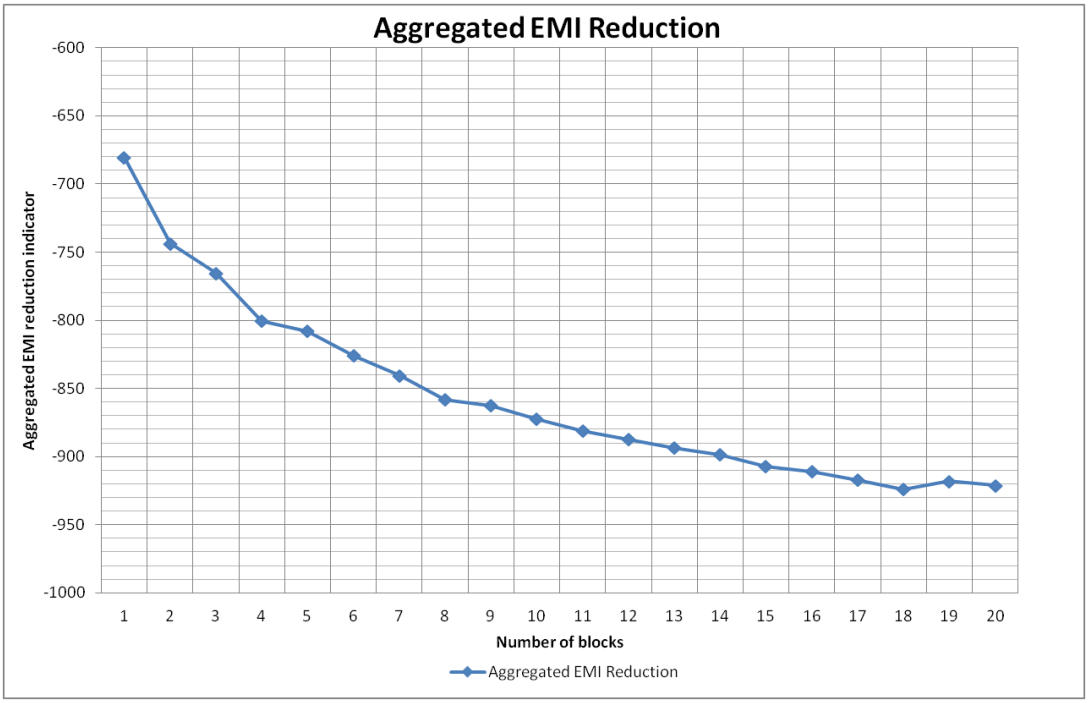

Figure 4.8. Aggregated EMI reduction for different GALS granularities. The indicator is calculated as a sum of EMI reductions across different frequency ranges

It can be seen that after partitioning with 15 different blocks that differences are insignificant and that EMI profile saturates. This can also be observed in Figure 4.7, where the different curves for different frequencies ranges are presented. There can be seen a saturation of EMI, in low frequency range, after 18 blocks, and in high frequency range already at GALS partitioning with 15 blocks. Achieved maximal reduction in low frequency range oscillated around 25 dB, and in a high frequency range - 22 dB. Finally, those results can be extrapolated to evaluate the possibilities for EMI reduction also for the pure asynchronous systems. Since it is observable that the system saturates after deeper partitioning, it can be generally estimated the EMI features of the asynchronous systems. Asynchronous system could be presented as GALS system with infinite number of GALS blocks, as in saturation it can be expected that it would behave similarly to GALS system.

4.3. Evaluation of solutions using jitter

The next important task was to investigate jitter impact on EMI reduction both in synchronous and corresponding GALS systems. The aim of such an investigation was to establish how the jitter parameters influence EMI reduction in digital circuits and GALS systems specifically. Thus, first synchronous systems has been investigated and then corresponding GALS systems in terms of a basic frequency. Both systems have been compared regarding EMI reduction with jittered clocks. Finally, the borders of EMI reduction with jittered clock signals has been investigated in order to find a way the jitter influence EMI in GALS (and synchronous) systems. The research was necessary in order to have a deep knowledge regarding EMI reduction with and without jitter using different parameters' settings. It was further used to set appropriate parameters for hybrid optimization.

All studies were performed with the same Monte Carlo method settings. Each simulation contained a series of 200 runs consisting of series of randomly applied current waveform shifted in time by a random jitter value in the predetermined range. The probability of selecting one out of five current profiles was 20%. Similarly, the probability of selecting a given value of jitter was uniformly distributed. Subsequently all the waveforms were subjected to averaging in order to obtain consistent results. Each of

those tests was conducted in 11 frequencies' ranges, in order to verify noise in wide spectrum and against different harmonics of the signal. To generate random sample an algorithm of "Mersenne twister" was used with a period of 2^{19937}-1.

4.3.1. 10 modules synchronous system

First of the examined systems had a star topology, and consisted of 10 modules clocked at 50 MHz. A simulation was performed for the selected eleven frequency ranges with an assumption that jitter will modify the base frequency in the range from 0 to 15% (Figure 4.9).

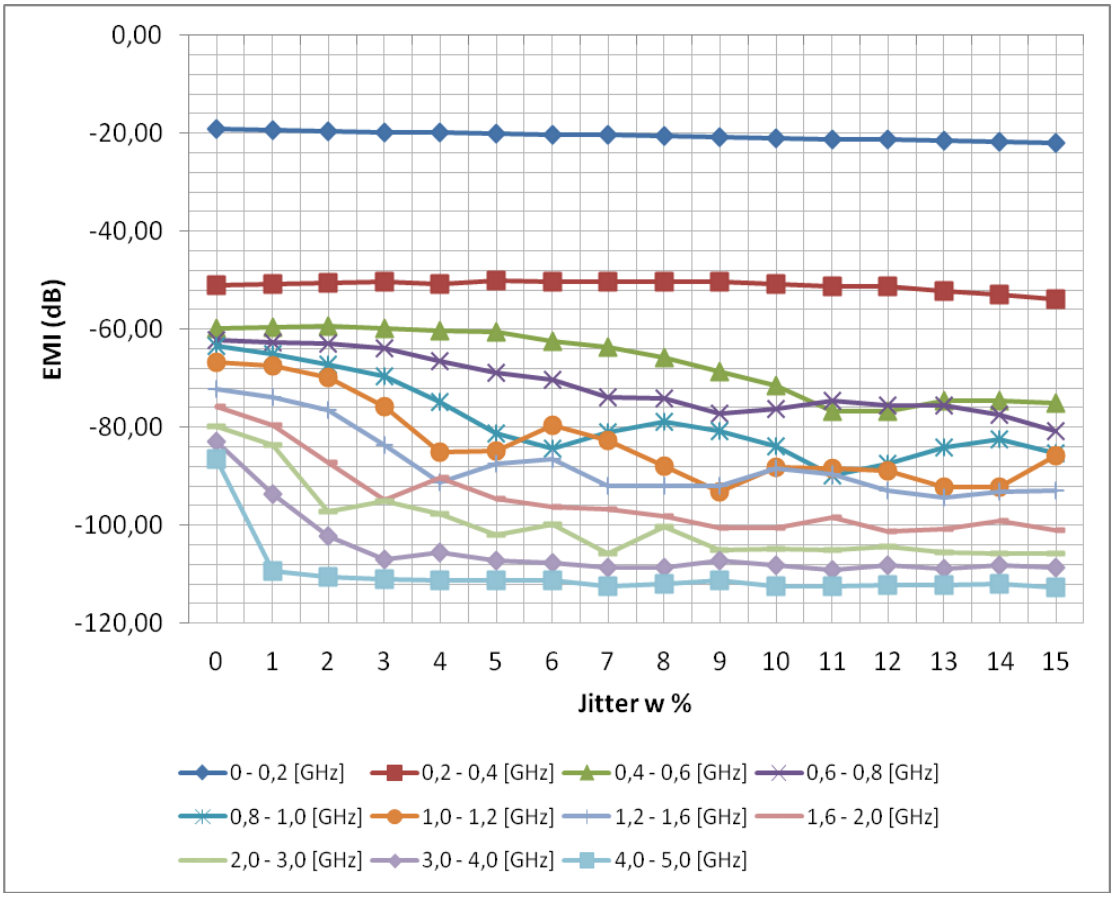

Figure 4.9. Simulation results of 10 modules star topology - synchronous system against EMI reduction with different values of applied jitter

It can be seen (Figure 4.9), that a significant reduction of EMI is visible in range of 1-10% jitter modification. Other ranges effect in none or very slight decrease of EMI reduction in all frequency bands. Additionally, it is evident that the lower frequencies are significantly less extinguished than the high ones. This is related to the fact that

jitter effects the higher frequencies much more by implementing minor phase fluctuations.

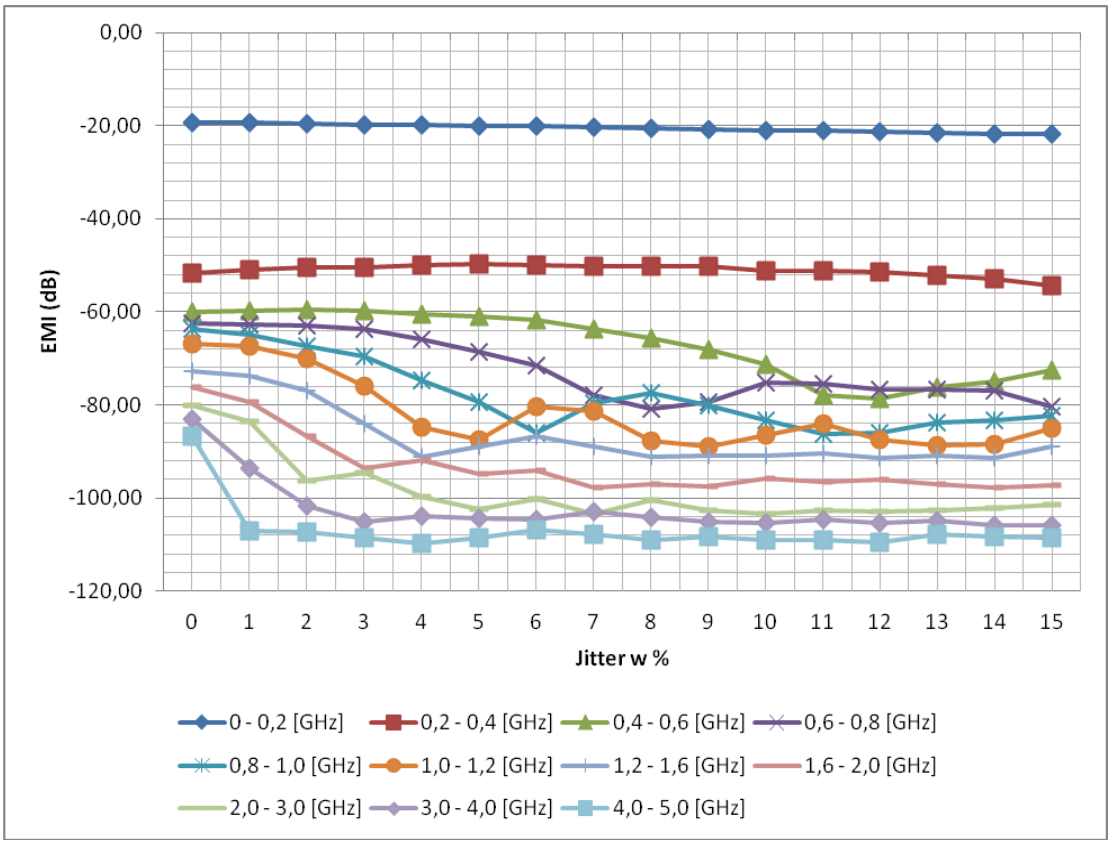

Figure 4.10. Simulation results of 4 modules star topology - synchronous system against EMI reduction with different values of applied jitter

4.3.2. 4 modules synchronous system

Next analyzed system had the star topology, and consisted of four modules clocked at 50 MHz. As in the previous scenario a simulation was performed for 16 settings of jitter from 0-15%. Likewise the previous simulation, it can be seen (Figure 4.10) that the suppress rate of a particular frequency depends on its range. Thus in the first place the higher ranges are muted. However, the lower ones have quite linear characteristic. This results directly from the fact that the lower frequencies would be suppressed much faster by, for example, 50% jitter. It can be achieved easier by a phase shift of each block; however, this is not an objective of this experiment.

4.3.3. 4 modules GALS system

In the third experiment a GALS system with 4 modules was analyzed. Each of modules had a different clock generator (46, 48, 50, 52 MHz). It can be noticed (Figure 4.11) that in the asynchronous GALS system the lower frequencies do not undergo practically any suppressing. This is due to the properties of such systems described before.

It is worth noticing here (that fact can be observed in Figures 4.10 and 4.11) that GALS system reduces EMI around 10dB better. It is caused by a fact that GALS by its nature – different frequencies - provide phase shift to each block.

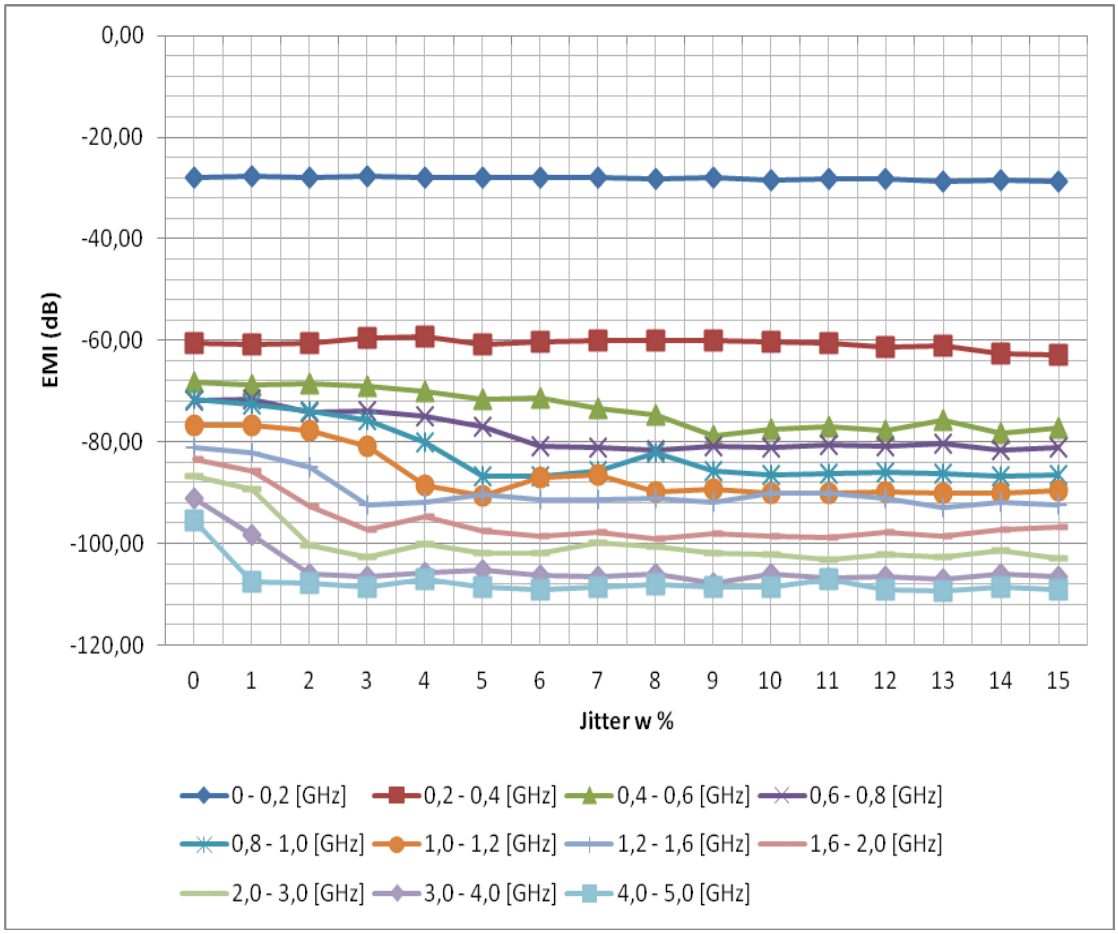

Figure 4.11. Simulation results of 4 modules star topology asynchronous system against EMI reduction with different values of applied jitter

GALS systems have stoppable clocks that generate phase shifts. This affects the dispersion of current peaks in time, thereby reducing noise in the lower frequencies.

However, a higher frequency of about 500 MHz, experience similar reductions, as it was in case of synchronous systems. The higher the frequency, the harder and faster they are suppressed according to the jitter level.

The borders of EMI reduction have been investigated in GALS systems. As a result, it has been shown that the optimum range of jitter parameters for different systems and different topologies are close to 10%. Increasing this parameter evidently does not affect further significant reduction in EMI. Additionally increasing this parameter might have a detrimental impact on a whole system by causing a number of errors during its operation. Furthermore, it was presented that the lower frequencies are significantly less, but more linearly reduced in terms of electromagnetic interference in synchronous systems. However, in the asynchronous GALS systems because of their characteristics, (different blocks' frequencies) jitter impacts only higher frequencies.

4.4. Comparison synchronous with GALS systems

In Figure 4.12 combinations of both systems with the best results are presented. A standard synchronous system, synchronous system with phase shift and jitter, and a GALS system with high block granularity and with jitter were selected for evaluation. It is noticeable that the results of the low-EMI synchronous system are slightly worse than the GALS system with the best EMI characteristic. In the low-EMI GALS system EMI is reduced around 26 dB compared to the classic synchronous approach.

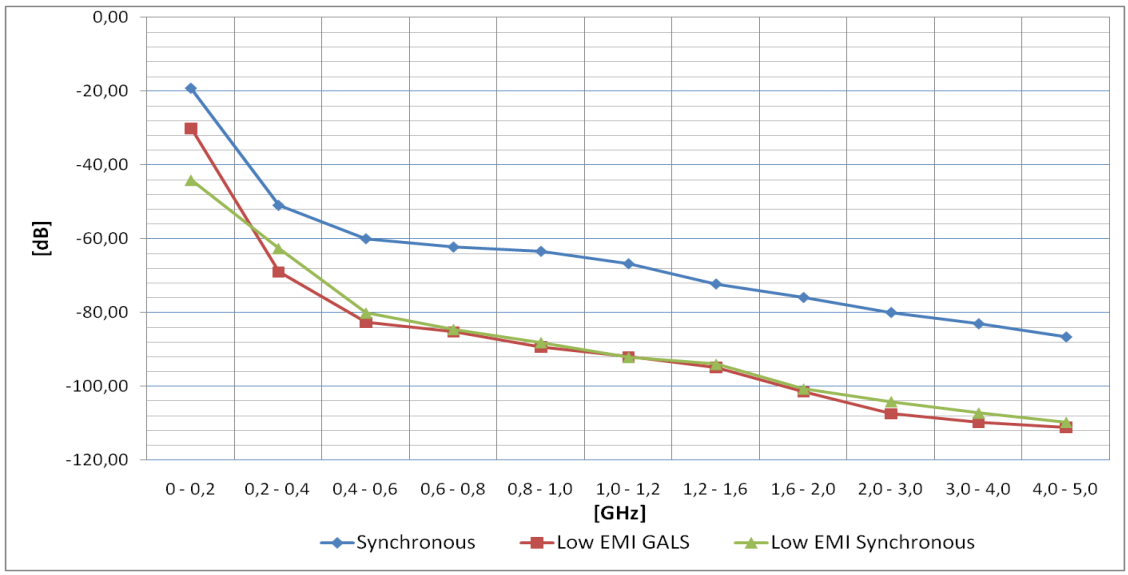

Figure 4.12. Comparing the best results from the Synchronous and GALS systems

If the differences are compared in time domain for the classic synchronous design, where maximal current supply is equal to 1A (Figure 4.13) in this research and the low-EMI GALS system (10 blocks, star topology with jitter), around 40% current peak reduction can be observed (Figure 4.16). When only jitter is applied to a synchronous system, reduction of current peaks, in time domain, is visible at around 10% (Figure 4.14). When a phase shift is also included to each sub-block of synchronous system, a 50% reduction of current peaks is possible (Figure 4.15). However, this kind of synchronous system modification is only theoretical, while in real-life scenarios it would be almost impossible to design such a system with current tools. Thus, GALS technology can provide a chip designers with reasonable solution regarding current peak reduction by utilizing its asynchronous features.

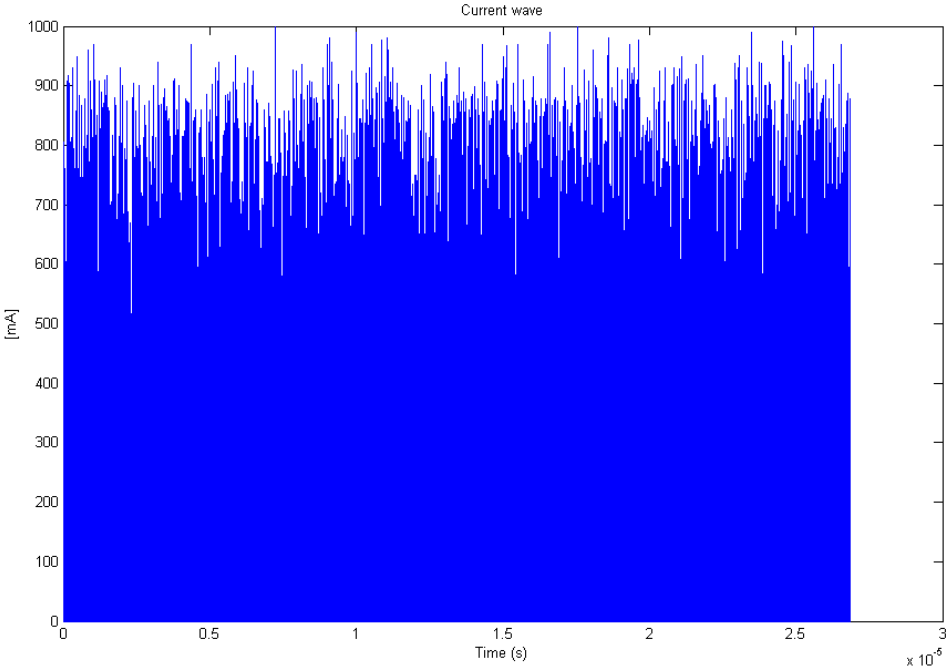

Figure 4.13. Current wave of 10-module synchronous star topology in time domain without jitter and phase shift

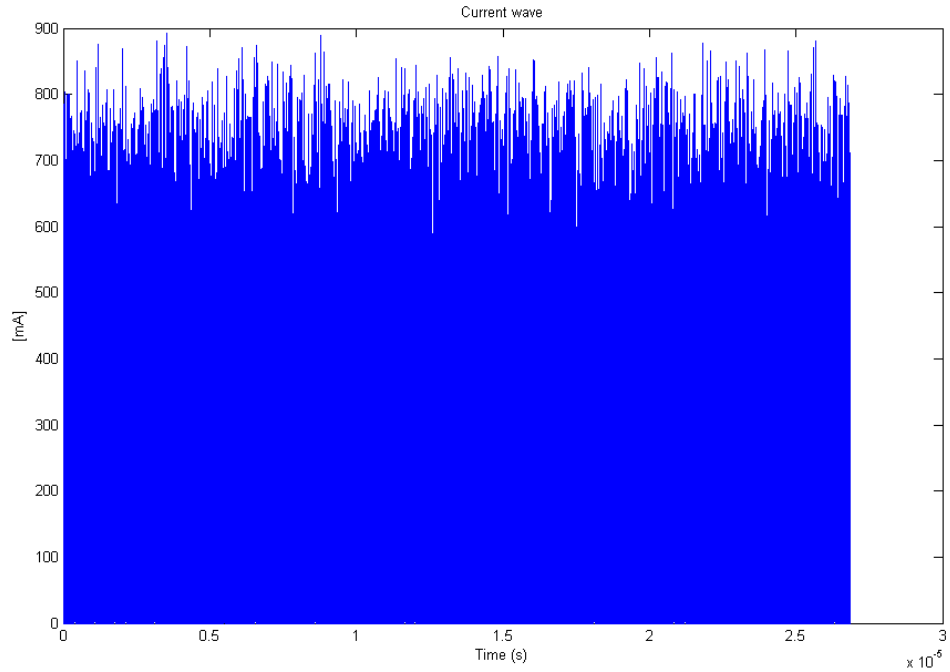

Figure 4.14. Current wave of 10-module synchronous star topology in time domain with 10% jitter and no phase shift

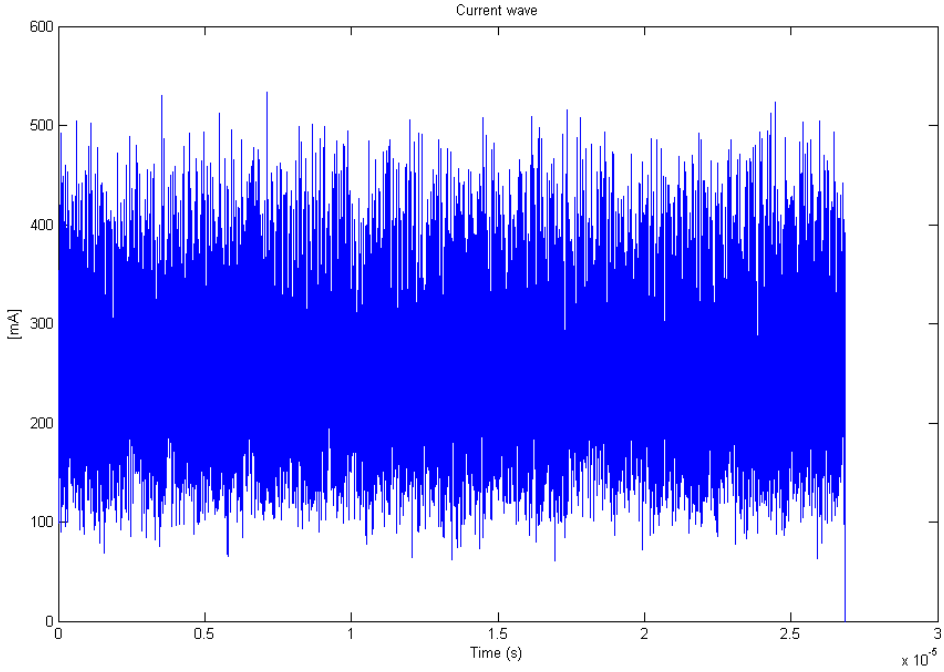

Figure 4.15. Current wave of 10-module synchronous star topology in time domain with 10% jitter and phase shift distributed evenly among blocks: 0, 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%

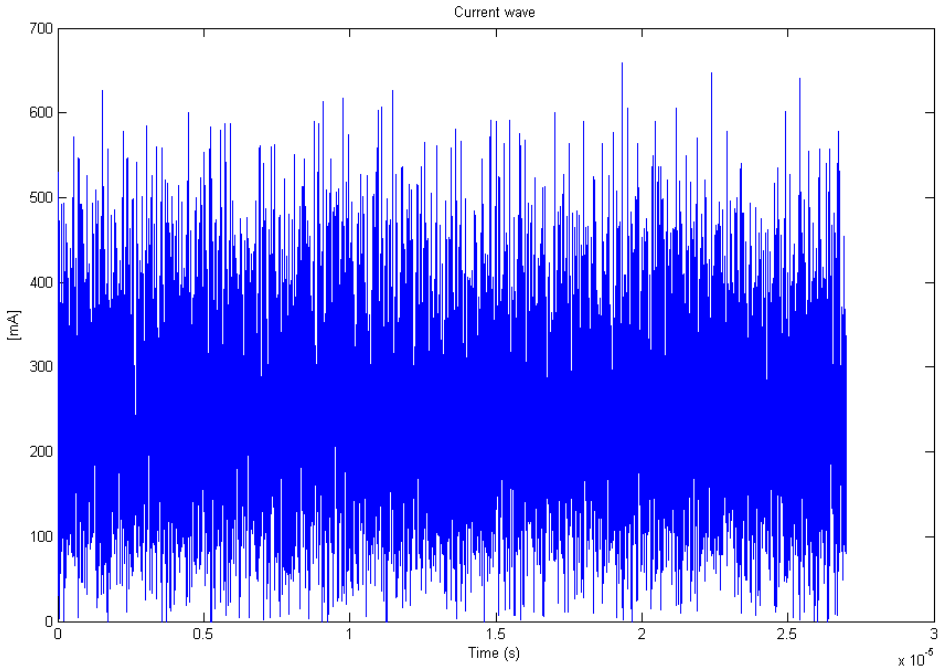

Figure 4.16. Current wave of 10-module GALS star topology in time domain with burst mode data transfer, medium spread frequencies (2) and 10% jitter

4.5. Hybrid optimization results

According to previous studies, the rules for selecting appropriate parameters of GALS systems are complicated. Those consist of selecting a huge number of parameters, where a little change can have a tremendous impact on EMI results: improving or declining the general EMI characteristic. The basic parameters (jitter, granulation) and their influence on EMI in GALS systems has been investigated throughout. However, accurate setting of blocks' frequencies is not a trivial task. Each block can differ with top power supply and searching the best set of frequencies within specified ranges could take ages with the previous simulator. In order to facilitate the process of selecting appropriate parameters of GALS systems, especially frequencies of each block, a hybrid optimization algorithm has been applied to the simulator. First step of hybrid optimization algorithm is to run a number of Monte Carlo simulations. The higher the number of runs the longer it takes, however, the ranges of specified frequencies are investigated throughout. Then the best result of Monte Carlo optimization is further optimized according to the direct search procedure. The second part of hybrid optimization algorithm searches the area of possible frequencies according to orthogonal vectors without changing directions and decreasing step (Hook-Jevees method). With 4 GALS blocks for instance, the vectors can be marked as an orthogonal vectors matrix with 8 vectors.

4.5.1. 4 blocks GALS system with different initial settings

GALS system, investigated against the hybrid optimization, consisted of 4 GALS blocks in a star topology. Each block could run in a range of frequencies between 47 and 53 Mhz. Jitter with LFSR has been applied to each block with parameters set to:

- Jitter up to 10% of clock length
- Resolution of 32
- Generated by LFSR with length of 15 bits

Current peaks of each block were set according to:

- 100 mA
- 400 mA
- 200 mA

- 300 mA

The aim was to establish the lowest possible EMI in such a GALS system by setting quasi-optimal frequencies within input ranges. The hybrid optimization algorithm consisted of dedicated number of steps of Monte Carlo optimization. It was followed by a direct search with an initial step of 1 MHz and correction of 0,1 in case of no further improvement with current step length. The results can be observed in Tables 4.15, 4.16 and Figure 4.17. The number of Monte Carlo iterations is set to 10.

Table 4.15. First part results of hybrid optimization with Monte Carlo simulation - 4 GALS blocks, 10 optimization iterations and applied jitter to each block

	Step number	1	2	4	5	10
Best frequencies	Block 1	51,88	52,38	52,67	47,13	50,71
	Block 2	52,43	50,61	50,9	49,54	51,22
	Block 3	47,76	48,55	48,16	48,8	49,61
	Block 4	52,48	50,49	48,95	52,2	47,53
Indicator		-87,396	-90,4037	-90,3449	-90,7406	-90,7649
Mean		-80,0356	-82,3434	-82,3675	-82,5418	-82,6456
Range of frequencies [GHz]	0 - 0,2	-22,2808	-26,2112	-26,0681	-27,5825	-26,5557
	0,2 - 0,4	-59,6245	-62,7721	-63,2688	-63,7334	-63,727
	0,4 - 0,6	-70,3524	-74,1916	-73,7516	-74,3512	-73,7522
	0,6 - 0,8	-77,1969	-78,5857	-77,7437	-77,8509	-78,7015
	0,8 - 1,0	-83,0219	-84,2293	-84,5553	-83,7775	-84,641
	1,0 - 1,2	-87,4013	-87,2781	-85,652	-87,0755	-87,26
	1,2 - 1,6	-85,2061	-89,7573	-89,5229	-89,2317	-90,346
	1,6 - 2,0	-94,5418	-95,3021	-95,383	-94,985	-95,6739
	2,0 - 3,0	-97,4859	-98,6828	-99,8573	-100,5785	-99,9969
	3,0 - 4,0	-103,1994	-103,5696	-104,4146	-104,3039	-103,6181
	4,0 - 5,0	-100,0811	-105,1981	-105,8251	-104,4897	-104,8295

Table 4.16. Results of second part of hybrid optimization with Direct Search (Hook-Jevees) optimization - 4 GALS blocks and applied jitter to each block

	Step number	1	2	3	4	5	6	7
Best frequencies	Block 1	step change	50,71	50,61	50,61	50,51	step change	50,51
	Block 2	0,1	51,22	51,22	51,12	51,12	0,01	51,13
	Block 3		49,61	49,61	49,61	49,61		49,61
	Block 4		47,63	47,63	47,63	47,63		47,63
Mean			-82,676	-82,714	-82,787	-82,826		-82,8639

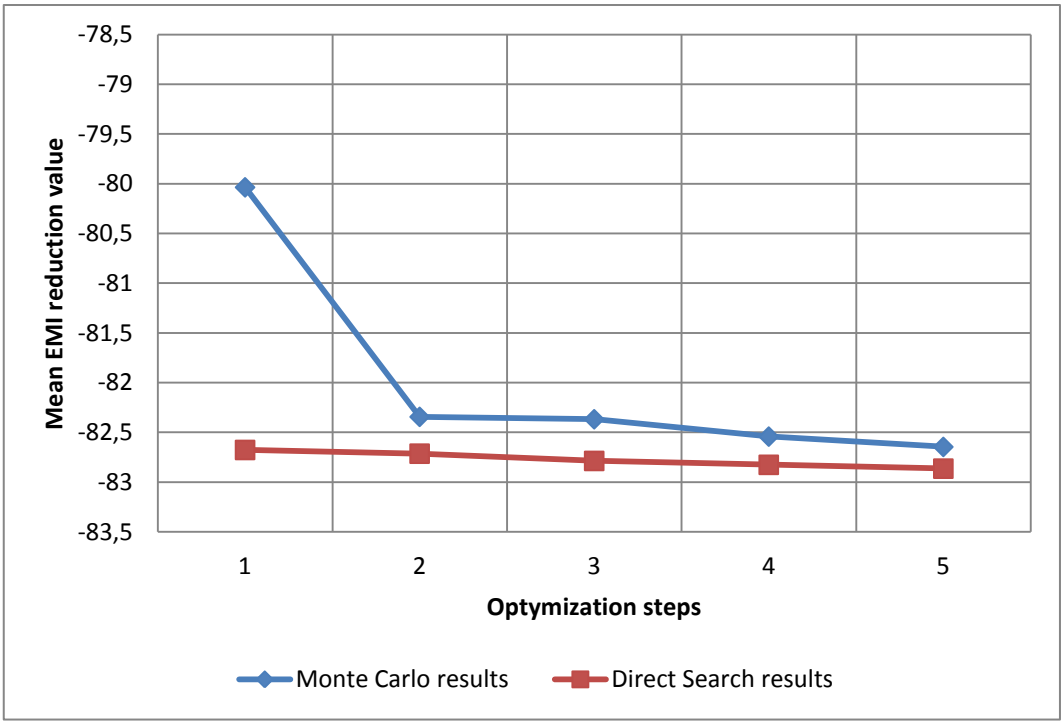

Figure 4.17. Results of hybrid optimization - 4 GALS blocks, 10 Monte Carlo optimization iterations and applied jitter to each block

It can be noticed that only 5 out of 10 Monte Carlo iterations gave a better result than a previous best solution. The objective function depends on the mean value of 11 range frequencies. Whereas the Monte Carlo method quickly finds a good result, the following direct search improves the result further.

Table 4.17. Results of hybrid optimization - 4 GALS blocks and applied jitter to each block, 100 Monte Carlo iterations

Step number		1	4	6	19	21	32	44	69	1
Best frequencies	Block 1	50	51,42	47,15	52,11	52,79	51,63	47,8	48,17	48,17
	Block 2	47,78	47,46	47,22	47,86	49,76	48,75	47,23	47,29	47,29
	Block 3	49,91	50,58	50,18	47,17	47,21	48,38	49,82	50,45	50,45
	Block 4	49,19	50,89	48,24	48,69	49,56	47,85	51	47,93	48,93
Indicator		-90,7401	-91,0455	-91,2046	-91,3989	-91,6239	-91,6103	-91,4472	-91,6068	-91,6103
Mean		-82,6837	-82,9058	-82,9331	-83,0566	-83,0645	-83,1206	-83,1641	-83,2138	-83,2603
Range of frequencies [GHz]	0 - 0,2	-25,9198	-26,9569	-27,8129	-28,3354	-31,3596	-30,2041	-28,3316	-29,1878	-28,6007
	0,2 - 0,4	-63,5634	-63,9329	-64,0829	-63,7918	-63,7446	-63,799	-63,5607	-64,0364	-63,7866
	0,4 - 0,6	-74,0921	-73,5121	-74,5321	-75,2668	-74,1943	-74,58	-74,389	-74,8094	-74,8868
	0,6 - 0,8	-78,7475	-79,0569	-78,8471	-78,7359	-78,6748	-79,0739	-79,5652	-78,9902	-79,5536
	0,8 - 1,0	-84,1702	-84,1222	-83,4273	-84,3668	-83,8809	-83,909	-84,2339	-83,6913	-84,3377
	1,0 - 1,2	-87,7142	-87,8503	-87,3107	-86,846	-87,304	-87,0949	-87,1631	-87,3602	-87,1102
	1,2 - 1,6	-90,7815	-90,6689	-90,7051	-90,9461	-89,386	-90,5003	-90,3276	-90,5815	-90,2629
	1,6 - 2,0	-95,8828	-96,253	-96,0202	-95,9277	-95,2808	-95,5029	-95,7415	-95,536	-95,6786
	2,0 - 3,0	-100,848	-99,94	-100,152	-99,4758	-100,08	-99,707	-100,645	-100,852	-100,671
	3,0 - 4,0	-104,622	-105,084	-104,499	-103,343	-104,199	-104,336	-104,614	-104,693	-104,906
	4,0 - 5,0	-103,179	-104,587	-104,874	-106,588	-105,606	-105,619	-106,233	-105,613	-106,07

In Table 4.17 it can be observed that by increasing the number of Monte Carlo iterations the indicated value of all measured frequencies improves. Moreover, Direct Search offers fewer steps, and sometimes allows getting a final result after only one step.

Figure 4.18 compares two instances of an objective function that can be applied. The first one is a mean value of measured EMI reduction from values at 11 ranges of frequencies. The second one is an indicator consisting of the same values at 11 ranges of frequencies but with weights. Presented here indicator focuses on the low frequencies. Hence, in some points of the figure it is notable that objective functions can differ. Although the mean value is lower, the low spectral ranges can be reduced less in term of EMI. It suggests that depending on the range that needs to be lowered against EMI, setting of weight in the indicator allows the proper optimization.

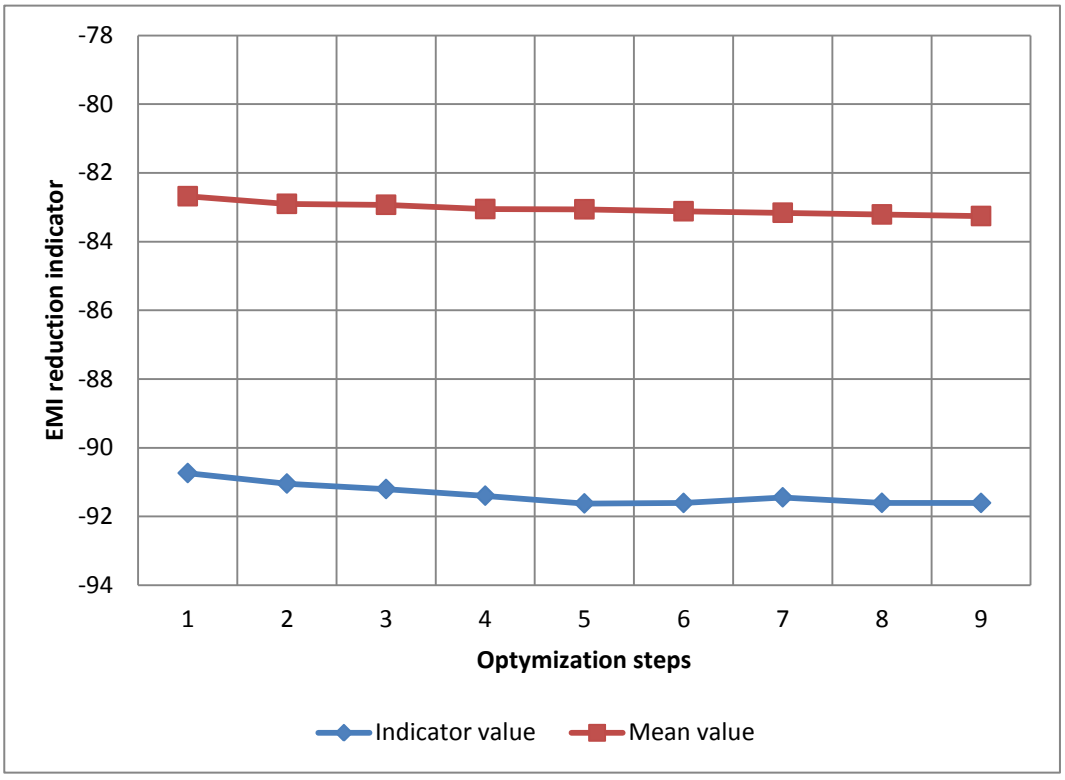

Figure 4.18. Results of hybrid optimization and 2 different indicators from Table 4.16. 4 GALS blocks, 100 Monte Carlo optimization iterations and jitter applied to each block

In order to verify a sufficient number of Monte Carlo iterations necessary to generate an acceptable results a series of simulations with 500 Monte Carlo iterations were run. It appears that the reasonable number of Monte Carlo iterations is around 100. Further increase only consumes more computing without generating better results. An instance of such simulation is presented in Table 4.18. A satisfactory result is generated in 55th iteration. Moreover, this result implicates no further improvement with second stage of hybrid optimization – Direct Search. It can be noticed that all of the simulations bring similar results.

Table 4.18. Sample results of hybrid optimization - 4 GALS blocks and jitter applied to each block, 500 Monte Carlo iterations

Step number		1	2	4	5	8	17	55
Best frequencies	Block 1	51,2	48,75	52,89	47,12	52,48	51,26	47,91
	Block 2	51,32	50,81	47,36	47,95	49,25	48,38	47,77
	Block 3	51,28	48,85	52,79	48,01	51,22	47,66	48,43
	Block 4	52,49	48,32	48,04	51,23	49,94	49,14	47,25
Indicator		-87,7389	-90,416	-90,4857	-90,8519	-91,0423	-91,3456	-91,8335
Mean		-80,4081	-82,4133	-82,4174	-82,765	-82,7818	-82,9925	-83,5107
Range of frequencies [GHz]	0 - 0,2	-22,852	-26,5149	-25,9141	-26,0149	-28,4445	-28,434	-28,5025
	0,2 - 0,4	-59,4891	-62,3826	-63,6475	-63,6494	-63,5844	-63,7453	-63,9906
	0,4 - 0,6	-72,3159	-73,5437	-74,2879	-74,1909	-74,135	-74,9537	-74,891
	0,6 - 0,8	-74,898	-78,6837	-78,7173	-79,1407	-78,2845	-78,9711	-79,389
	0,8 - 1,0	-83,5421	-83,9303	-83,1658	-84,5178	-83,9114	-84,2721	-84,5832
	1,0 - 1,2	-85,2518	-87,4116	-86,7565	-87,1944	-87,6129	-87,4641	-87,5212
	1,2 - 1,6	-88,6419	-90,144	-89,5985	-90,1184	-89,3534	-90,2767	-90,9018
	1,6 - 2,0	-93,6621	-95,4865	-95,3264	-96,1421	-95,2941	-95,5691	-96,2603
	2,0 - 3,0	-99,3469	-99,991	-99,985	-99,89	-100,198	-100,317	-100,891
	3,0 - 4,0	-103,147	-104,051	-104,309	-103,571	-104,53	-104,311	-104,623
	4,0 - 5,0	-101,343	-104,407	-104,883	-105,986	-105,252	-104,604	-107,065

Finally, a GALS system without jitter was investigated against EMI reduction by hybrid optimization. In Tables 4.19, 4.20 and Figure 4.19 all the results are presented. It can be noticed that similarly to previous investigations the schema of working for hybrid optimization is comparable but caused by the lack of jitter application the results are worse. First the Monte Carlo brings good results within 4 steps and then Direct Search improves it more in 3 full steps.

Table 4.19. Results of first part of hybrid optimization with Monte Carlo simulation - 4 GALS blocks, 100 optimization iterations and no jitter

Step number		1	2	5	12
Best frequencies	Block 1	50,57	51,93	52,92	52,15
	Block 2	50,99	49,88	47	48,17
	Block 3	49,19	47,2	47,51	49,39
	Block 4	50,35	51,48	49,97	50,03
Indicator		-79,3645	-80,6249	-81,0779	-80,9696
Mean		-71,635	-72,7238	-72,9351	-72,9954
Range of frequencies [GHz]	0 - 0,2	-25,2815	-24,9079	-28,2715	-26,4208
	0,2 - 0,4	-61,7841	-62,6405	-63,4798	-62,9287
	0,4 - 0,6	-64,8603	-67,4914	-65,8869	-66,4811
	0,6 - 0,8	-67,4888	-67,792	-67,454	-68,9622
	0,8 - 1,0	-69,2661	-72,3293	-71,1104	-69,639
	1,0 - 1,2	-72,7709	-73,5566	-74,6623	-75,335
	1,2 - 1,6	-78,6971	-81,7605	-81,0608	-80,9643
	1,6 - 2,0	-81,6613	-83,4072	-83,2272	-81,594
	2,0 - 3,0	-85,6647	-84,8584	-84,4028	-86,06
	3,0 - 4,0	-88,8607	-89,197	-90,1704	-89,8158
	4,0 - 5,0	-91,6491	-92,0208	-92,5603	-94,7486

Table 4.20. Results of second part of hybrid optimization with Direct Search optimization - 4 GALS blocks, 100 optimization iterations and no jitter

Step number		1	2	3	4	5
Best frequencies	Block 1	52,15	step change	52,15	step change	52,15
	Block 2	48,17	0,1	48,17	0,01	48,17
	Block 3	49,39		49,39		49,39
	Block 4	49,03		49,13		49,14
Indicator		-81,0861		-81,2414		-81,2472
Mean		-73,0325		-73,1414		-73,1556
Range of frequencies [GHz]	0 - 0,2	-26,5022		-26,3685		-26,3565
	0,2 - 0,4	-63,3134		-63,835		-63,7846
	0,4 - 0,6	-66,4268		-66,5673		-66,4732
	0,6 - 0,8	-69,8621		-70,2966		-70,3726
	0,8 - 1,0	-69,5961		-69,6482		-69,6011
	1,0 - 1,2	-75,4326		-74,7448		-74,8792
	1,2 - 1,6	-79,8037		-80,7967		-80,8706
	1,6 - 2,0	-81,5455		-81,4934		-81,5447
	2,0 - 3,0	-86,112		-86,0911		-86,0813
	3,0 - 4,0	-89,8806		-89,8933		-89,852
	4,0 - 5,0	-94,8828		-94,8204		-94,8959

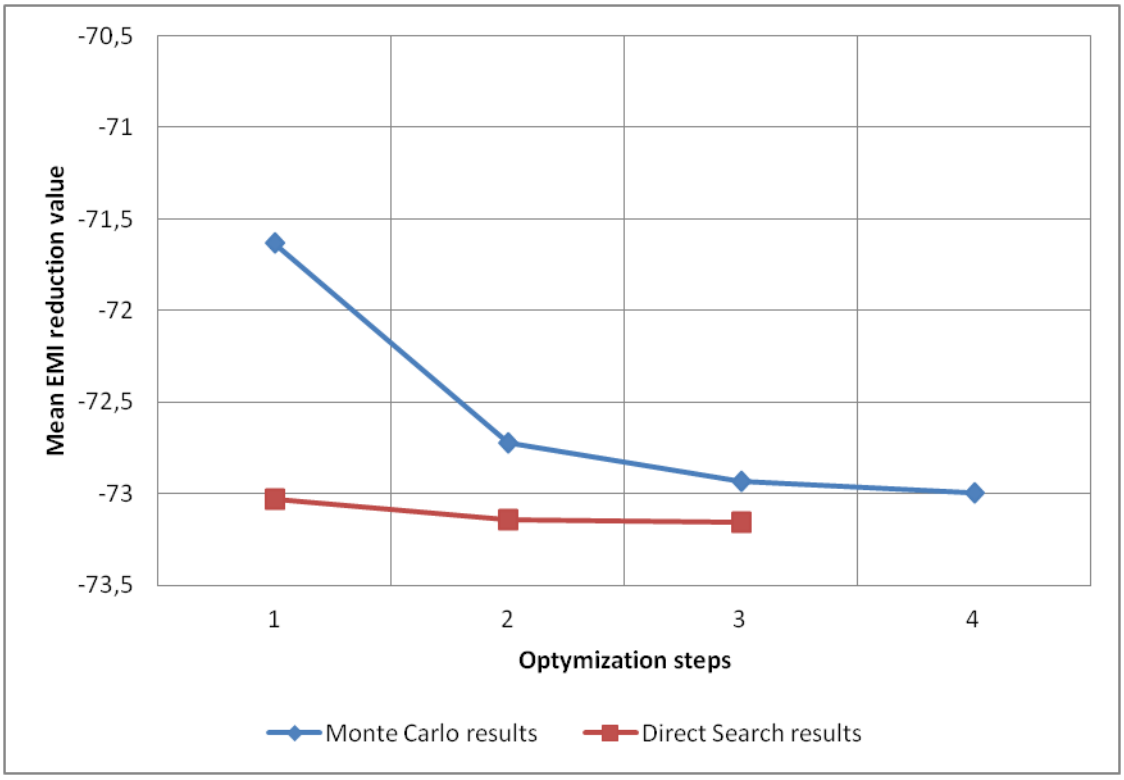

Figure 4.19. Results of hybrid optimization - 4 GALS blocks, 100 Monte Carlo optimization iterations and no jitter

To sum up, it can be stated that the hybrid optimization gives a good result in terms of EMI reduction in GALS systems regarding frequency selecting. The results are satisfactory regardless of the jitter application. In some ranges of frequencies the results can be improved by up to 6dB when comparing to manual search and around 20 dB comparing to a 4 module synchronous system. These values are great in terms of EMI reduction in a 4 module system and the presented algorithm is easily applicable to any other GALS system.

5. Summary

The possibility of EMI reduction in modern digital circuits' structures, called GALS (*Globally Asynchronous Locally Synchronous*) was the main objective of this dissertation. GALS is understood as a specific clock control schema and a special integration of various blocks of digital system in order to reduce the effect of EMI. GALS's practical implementation uses electronic circuits called jitter - its effect can be understood as the clock pulse width modulation. GALS approach also indicates a phase shift among GALS sub-block's clocking signals. Therefore, it is possible for every individual block's clocking system to work with different frequency. As a result of introducing GALS structure, it becomes possible to reduce EMI. This can subsequently reduce the possibility of errors occurrence in the next generation processor systems miniaturization.

In practical terms this allows to reduce the peak power value of the main computing system and preserve the same processing power by adjusting its structure to GALS architecture. It could also allow to build a computing system with more processing power while the main power supply is preserved. These features of GALS systems should be considered simultaneously with a reduction in probability of error occurrences in such a system. It is a practical and important advantage of applying GALS scheme.

Quantum computers are currently the only other well known solution to the problem of increasing processing power when the main power remains unchanged. Such computers can only perform at a temperature around absolute zero and are at a very preliminary stage; currently those are only used in the U.S. .

Initial research presented in this dissertation has been conducted in IHP (Innovations for High Performance Microelectronics) under the supervision of Dr. Milos Krstic [25]. First version of GalsEmilator has been created there. A software tool based on Matlab has been developed and evaluated in order to simulate EMI properties of the digital GALS systems. It supported simulations of GALS/synchronous systems with different granularity, frequencies, current shapes, topology, and other parameters.

Moreover, basic research has been conducted in IHP regarding EMI reduction among synchronous and GALS systems.

Further work has been completed in cooperation with IHP and Dr. Milos Krstic during author's practice training in NTT laboratories (Nippon Telegraph and Telecommunications), Japan, Kanagawa. Impact of system granularity on EMI reduction has been investigated and presented.

Final work has been completed at West Pomeranian University of Technology (Computer Science faculty). An indepth research concerning jitter impact has been conducted. Moreover, a hybrid optimization algorithm has been proposed to automate the whole process and support designers in decision making process of selecting appropriate frequencies of GALS blocks.

Using the software, different GALS and synchronous systems have been modeled in order to evaluate different topologies, architectures and EMI reduction techniques. It has also facilitated comparison of GALS and Synchronous systems.

The results show that the reduction of high spectral components can be successfully achieved with jitter introduction. EMI at low frequencies can be reduced by a phase shift applied for synchronous systems. However, combining those two features would be difficult in synchronous systems because of data transfer between blocks. In GALS circuits, phase shift is already incorporated by the nature of the GALS methodology. Moreover, it was discovered that a local clock generator, based on a ring oscillator, naturally generates a clock with jitter. However, this feature was not investigated in depth. In this work, an explicit jitter was introduced with the special jitter generators based on LFSR structures. By adding jitter in a GALS system, a significant reduction over whole spectrum is achievable, not affecting the functionality of a system. The reduction up to 26 dB is achievable, as illustrated in the results.

The results have been confirmed by GALS FFT processor produced in IHP and described before. Moreover, a second ASIC called Moonrake [26] has been designed and produced to verify EMI reduction in GALS systems. It also proved that the EMI can be reduced in GALS systems up to 26 dB, what is presented in this dissertation. It is worth noticing that both simulations and ASIC verification have been conducted separately leading to the same conclusions. It proves that the simulation model is well designed and executed. However, the developed tool to model EMI reduction has a much

wider possibilities to predict EMI in digital systems than the created and investigated processors produced in IHP.

Moreover, the current peaks in time domain can be reduced up to 40% by GALS systems. Similar results have been achieved in a real GALS processor [3]. Furthermore, it has found that there is almost no correlation between EMI reduction and data transfer intensity (i.e. clock pausing rate) in GALS modules. Used set of frequencies and the granularity of GALS partitioning has the greatest impact. Hybrid optimization algorithm confirmed that it is possible for further reduction of EMI comparing to a manual parameters setting.

Comparing low-EMI synchronous solutions and GALS methods, it can be concluded that low-EMI GALS approach gives better results than synchronous approach. Finally, the whole process of selecting appropriate values, especially blocks' frequencies can be automated in order to facilitate designers of digital components.

Further work will focus on evaluating more real systems and comparing the simulation results with other real measured EMI values for GALS and synchronous implementations.

Subject of dissertation: Technical Sciences

Discipline of dissertation: Computer Science

ACM classification:

Software and its engineering

Software creation and management

Software development process management

Risk management

Information systems

Information systems applications

Decision support systems

Expert systems, Data analytics

References

[1] E. Grass, F. Winkler, M. Krstić, A. Julius, C. Stahl, M. Piz, Enhanced *GALS Techniques for Data path Applications*, Proc. of PATMOS, LCNS 3728, Springer Verlag, pp. 581-590, Leuven, Belgium 2005.

[2] S.B. Furber, et al, AMULET2e*: An Asynchronous Embedded Controller*, Proceedings of the IEEE, volume 87, number 2, pp. 243-256, ISSN 0018-9219, February 1999.

[3] M. Krstić, E. Grass, and C. Stahl, *Request-driven GALS Technique for Wireless Communication System*, Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems, March 2005, pp. 76–85.

[4] M. Krstić, E. Grass, C. Stahl, M. Piz, *System Integration by Request-driven GALS Design*, IEEE Proc. Computers & Digital Techniques, Vol 153, Issue 5, September 2006, pp. 362-372.

[5] H-S Kim, *Impact of Scaling on the Effectiveness of Dynamic Power Reduction Schemes*, Proceedings of the 2002 IEEE International Conference on Computer Design: VLSI in Computers and Processors (ICCD'02), p.382, September 16-18, 2002

[6] M. Badaroglu, K. Tiri, G. Van der Plas, P. Wambacq, I. Verbauwhede, S. Donnay, G.G.E Gielen, H.J. De Man, *Clock-skew-optimization methodology for substrate-noise reduction with supply-current folding,* Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Volume 25, Issue 6, June 2006, pp.1146 – 1154.

[7] J. Muttersbach, *Globally-Asynchronous Locally-Synchronous Architectures for VLSI Systems*, Doctor of Technical Sciences Dissertation, ETH Zurich, Switzerland, 2001.

[8] J. Muttersbach, T. Villiger, W.Fichtner: *Practical Design of Globall-Asynchronous Locally-Synchronous Systems,* Proc. of ASYNC'00, Eilat, Israel, pp. 52-59, 2000.

[9] E. Beigne, P.Vivet, *Design of On-chip and Off-chip Interfaces for a GALS NoC Architecture,* Proc. of ASYNC'06, Grenoble, France, pp 172-181, March 2006.

[10] M. Badaroglu et al., *Digital ground bounce reduction by phase modulation of the clock*, Proceedings Design, Automation, and Test in Europe (DATE) Conference (2004), Vol. 1, p. 10088.

[11] T. Król, M. Krstic, X. Fan, E. Grass, *Modeling and Reducing EMI in GALS and Synchronous Systems*, Integrated Circuit and System Design, Power and Timing Modeling, Optimization and Simulation, Springer, Lecture Notes in Computer Science, 2010, Volume 5953/2010, 146-155.

[12] K.A. Jenkins, J. Lo, P. Song, T. Xia, *Programmable Jitter Signal Generator*, United States Patent, Patent No.: US 7,095,264 B2, Date of Patent: August 22 2006.

[13] S.F. Smith, *An Asynchronous GALS Interface with Applications*, In Proceedings of the IEEE Workshop on Microelectronics and Electron Devices, 2004, pp. 41–44.

[14] A. Chattopadhyay and Z. Zilic, *GALDS: A Complete Framework for Designing Multiclock ASICs and SoCs*, IEEE Transactions on VLSI Systems 13 (2005), no. 6, 641–654.

[15] J. Kessels, A. Peeters, P. Wielage, and S. Kim, *Clock Synchronization through Handshake Signalling*, Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems, April 2002, pp. 59–68.

[16] S. Moore, G. Taylor, R. Mullins, and P. Robinson, *Point to Point GALS Interconnect*, Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems, April 2002, pp. 69–75.

[17] D.S. Bormann and P.Y.K. Cheung, *Asynchronous Wrapper for Heterogeneous Systems*, Proc. International Conf. Computer Design (ICCD), October 1997.

[18] F.K. Gürkaynak, *GALS System Design: Side Channel Attack Secure Cryptographic Accelerators,* doctoral thesis, published by ETH, Zürich 2006.

[19] T.X.P. Song, K.A. Jenkins, J. Lo. *Delay Chain Based Programmable Jitter Generator.* Proceedings of the Ninth IEEE European Test Symposium (ETS'04) 2004.

[20] T. Król, *Globally Asynchronous Locally Synchronous Interfaces Applied for EMI Reduction*, master thesis, West Pomeranian University of Technology, Computer Science faculty, 2009

[21] http://elektronikab2b.pl/technika/9588-redukcja-interferencji-elektromagnetycznych?start=1#.Uo0lRuLjWPA (12.02.2014)

[22] M. Krstic, T. Krol, X. Fan, E. Grass (IHP), "*Report on EMI reduction with GALS*", 31. Jul. 09.
(http://www.galaxy-project.org/files/D11_IHP_rev2_Report%20on%20EMI%20reduction.pdf)

[23] Xin Fan ; IHP Microelectron., Frankfurt (Oder), Germany ; Krstic, M. ; Wolf, C. ; Grass, E., *A GALS FFT processor with clock modulation for low-EMI applications*, Application-specific Systems Architectures and Processors (ASAP), 2010 21st IEEE International Conference on, Page(s): 273 - 278 , ISBN: 978-1-4244-6966-6

[24] http://users.rcn.com/wpacino/jitwtutr/jitwtutr.htm (12.02.2014)

[25] http://www.ihp-microelectronics.com/en/research/system-design/design-test-methodology.html (12.02.2014)

[26] Krstic, M., Fan, X. ; Grass, E. ; Heer, C. ; Sanders, B. ; Benini, L. ; Kakoee, M.R. ; Strano, A. ; Bertozzi, D. *Moonrake chip - GALS demonstrator in 40 nm CMOS technology,* System on Chip (SoC), 2011 International Symposium on, Oct. 31 2011-Nov. 2 2011, Pages: 9 – 13, Print ISBN: 978-1-4577-0671-4

[27] M. Krstic. T. Krol, X. Fan, E. Grass, *Reducing EMI using GALS Approach*, Journal of Low Power Electronics (JOLPE), Volume 6, Number 1, April 2010 , pp. 181-191(11).

[28] Xin Jia ; Cincinnati Univ., OH, USA ; Vemuri, R, *The GAPLA: a globally asynchronous locally synchronous FPGA architecture,* Published in: Field-Programmable Custom Computing Machines, 2005. FCCM 2005. 13th Annual IEEE Symposium on, 18-20 April 2005, Page(s): 291 – 292, Print ISBN: 0-7695-2445-1

[29] A. Royal, P. Y. K. *Cheung, Globally Asynchronous Locally Synchronous FPGA Architectures*, Field Programmable Logic and Application, Lecture Notes in Computer Science Volume 2778, 2003, pp 355-364

[30] G. Budzyń, *Programmable Logic Design, Lecture 10: FPGA clocking schemes, www.ue.pwr.wroc.pl/pld/pld_10.pdf* (12.02.2014)

[31] T. Xia, J. Campbell, J. Li, R. Wolf, J. F. Sweeney, *Jitter measurement circuit for mixed signal production test*, Measurement, Volume 40, Issue 3, April 2007, Pages 272–282, http://www.sciencedirect.com/science/article/pii/S0263224106001175?np=y (12.02.2014)

[32] A. Iyer , D. Marculescu, *Power and performance evaluation of globally asynchronous locally synchronous processors*, Proceedings of the 29th annual international symposium on Computer architecture, May 25-29, 2002, Anchorage, Alaska 2

[33] I. Blunno, C. Passerone, and G. A. Narboni, *An automated methodology for low electromagnetic emissions digital circuits design*. Proceedings of Euromicro Conference on Digital System Design (DSD), (2004), pp. 540–547.4

[34] R. Mullins , S. Moore, Demystifying Data-Driven and Pausible Clocking Schemes, Proceedings of the 13th IEEE International Symposium on Asynchronous Circuits and Systems, p.175-185, March 12-14, 2007

[35] F. K. Gurkaynak , S. Oetiker , H. Kaeslin , N. Felber , W. Fichtner*, GALS at ETH Zurich: Success or Failure*, Proceedings of the 12th IEEE International Symposium on Asynchronous Circuits and Systems, p.150, March 13-15, 2006

[36] E. Talpes , D. Marculescu, *Toward a multiple clock/voltage island design style for power-aware processors*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, v.13 n.5, p.591-603, May 2005

[37] F. K. Gurkaynak, S. Oetiker, T. Villiger, N. Felber, H. Kaeslin, and W. Fichtner, "*On the GALS design methodology of ETH Zurich*", in Proc. 1st Intl. Workshop For-

mal Methods for Globally Asynchronous Locally Synchronous Architecture (FMGALS), 2003.

[38] Siguenza-Tortosa, D.A.; Nurmi, J. "*Topology design for global link optimization in application specific network-on-chips*", System-on-Chip, 2004. Proceedings. 2004 International Symposium on, On page(s): 135 - 138

[39] P. Teehan , M. Greenstreet , G. Lemieux, *A Survey and Taxonomy of GALS Design Styles*, IEEE Design & Test, v.24 n.5, p.418-428, September 2007

[40] D. Ludovici , A. Strano , G. N. Gaydadjiev , D. Bertozzi, *Mesochronous NoC technology for power-efficient GALS MPSoCs*, Proceedings of the Fifth International Workshop on Interconnection Network Architecture: On-Chip, Multi-Chip, p.27-30, January 23-23, 2011, Heraklion, Greece

[41] Y. Thonnart , E. Beigné , A. Valentian , P. Vivet*, Power reduction of asynchronous logic circuits using activity detection*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, v.17 n.7, p.893-906, July 2009

[42] Xu-Guang Guan , Xing-Yuan Tong , Yin-Tang Yang, *Quasi delay-insensitive high speed two-phase protocol asynchronous wrapper for network on chips*, Journal of Computer Science and Technology, v.25 n.5, p.1092-1100, September 2010

[43] X. Fan , M. Krstić , E. Grass, *Analysis and optimization of pausible clocking based GALS design,* Proceedings of the 2009 IEEE international conference on Computer design, October 04-07, 2009, Lake Tahoe, California, USA

[44] A. Chattopadhyay and Z. Zilic. GALDS*: A Complete Framework for Designing Multiclock ASICs and SoCs*. IEEE Transactions on VLSI Systems, 13(6):641-654, June 2005.

[45] X. Fan, M. Krstić, E. Grass, B. Sanders, C. Heer, *Exploring pausible clocking based GALS design for 40-nm system integration*, Proceeding, DATE '12 Proceedings of the Conference on Design, Automation and Test in Europe, Pages 1118-1121, EDA Consortium San Jose, CA, USA ©2012

[46] E. Beigne et al., *Dynamic voltage and frequency scaling architecture for units integration within a GALS NoC*. Proceedings of International Symposium on Networks-on-Chip (2008), pp. 129–138.

[47] Li, N.; Ikeda, M.; Asada, K. "*Analysis of low noise three-phase asynchronous data transmission*", Solid-State Circuits Conference, 2005. ESSCIRC 2005. Proceedings of the 31st European, On page(s): 479 - 482

[48] Smith, S.F. "*An asynchronous GALS interface with applications*", Microelectronics and Electron Devices, 2004 IEEE Workshop on, On page(s): 41 - 44

[49] M. Krstić , E. Grass , F. K. Gürkaynak , P. Vivet, *Globally Asynchronous, Locally Synchronous Circuits: Overview and Outlook*, IEEE Design & Test, v.24 n.5, p.430-441, September 2007

[50] A. Hemani , T. Meincke , S. Kumar , A. Postula , T. Olsson , P. Nilsson , J. Oberg , P. Ellervee , D. Lundqvist, *Lowering power consumption in clock by using globally asynchronous locally synchronous design style*, Proceedings of the 36th annual ACM/IEEE Design Automation Conference, p.873-878, June 21-25, 1999, New Orleans, Louisiana, USA

[51] H.W. Ott, *Noise Reduction Techniques in Electronic Systems*, New York N.Y.: J. Wiley and Sons, 1988.

[52] A. Yakovlev , P. Vivet , M. Renaudin, *Advances in asynchronous logic: from principles to GALS & NoC, recent industry applications, and commercial CAD tools*, Proceedings of the Conference on Design, Automation and Test in Europe, March 18-22, 2013, Grenoble, France

[53] S. Sunter, A. Roy, *On-chip jitter measurement: from megahertz to giga-hertz*, IEEE Design and Test of Computers, (2004) 314–321.

[54] K. Niyogi and D. Marculescu, *System level power and performance modeling of GALS point-to-point communication interfaces*. Proceedings of the 2005 International Symposium on Low Power Electronics and Design (ISLPED) (2005), pp. 381–386.

[55] T. Osterman, B. Deutschman and C. Bacher, *Influence of the Power Supply on the Radiated Electromagnetic Emission of Integrated Circuits*, Microelectronics Journal 35 (Jun 2004), 525-530.

[56] J. Kim, D.G. Kam, P.J. Jun and J. Kim, *Spread Spectrum Clock Generator with Delay Cell Array to Reduce Electromagnetic Interference*, IEEE Trans. on Electromagnetic Compatibility 47 (Nov 2005), 908-920.

[57] H.-R. Cha and O.-K. Kwon, *An Analytical Model of Simultaneous Switching Noise in CMOS Systems*, IEEE Trans. on Advanced Packaging 23 (Feb. 2000), 62-68.

[58] W. Belardi and D. Pandini, *Analysis of the Clock Distribution Impact on EMI for EMC-Aware Clock-Tree Synthesis*, in Proc. EMC COMPO, Nov. 2007, pp. 109-114.

[59] M. Shimanouchi, *An approach to consistent jitter modeling for various jitter aspects and measurement methods*, ITC, Proceedings (2001) 848–857.

[60] T. Villiger, H. Kaeslin, F. K. Gürkaynak, S. Oetiker, and W. Fichtner. *Self-Timed Ring for Globally-Asynchronous Locally-Synchronous Systems*. In Proc. International. Symposium on Advanced Research in Asynchronous Circuits and Systems, pages 141-150, May 2003.

[61] Xin Wang; Ahonen, T.; Nurmi, J. "*A synthesizable RTL design of asynchronous FIFO*", System-on-Chip, 2004. Proceedings. 2004 International Symposium on, On page(s): 123 - 128

[62] J. Fernandes , M. Koutny , M. Pietkiewicz-Koutny , D. Sokolov , A. Yakovlev, *Step persistence in the design of GALS systems*, Proceedings of the 34th international conference on Application and Theory of Petri Nets and Concurrency, June 24-28, 2013, Milan, Italy

[63] Kenneth S. Stevens , Daniel Gebhardt , Junbok You , Yang Xu , Vikas Vij , Shomit Das , Krishnaji Desai, *The Future of Formal Methods and GALS Design*, Electronic Notes in Theoretical Computer Science (ENTCS), 245, p.115-134, August, 2009

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Streszczenie w języku polskim

Dysertacja ta (napisana w języku angielskim, ze względu na szerokie międzynarodowe grono potencjalnie zainteresowanych) dotyczy badań nad możliwościami redukcji interferencji elektromagnetycznej (EMI) w układach cyfrowych Globalnie Asynchronicznych Lokalnie Synchronicznych (GALS). Zjawisko EMI jest obecnie jedną z głównych przyczyn powstawania błędów w systemach cyfrowych przy zastosowaniu coraz mniejszych technologii wytwarzania procesorów (dochodzimy obecnie do technologii 14 nm i ciągle pracujemy nad ich dalszym zmniejszaniem). Redukcja EMI pozwala na dalsze wykorzystywanie dostępnych technologii produkcji układów cyfrowych, a przy tym tworzenie szybszych układów przy zredukowanej ich wielkości.

Na początku pracy, na podstawie dostępnej literatury, przedstawione i opisane zostały systemy GALS, obecne metody ich budowy, wykorzystywane elementy do ich tworzenia, sposoby komunikacji poszczególnych bloków oraz zalety wynikającego z takiego podejścia. Ponadto omówione zostały przyczyny powstawania interferencji elektromagnetycznej w układach cyfrowych, techniki analizy i modelowania EMI oraz dostępne metody jej redukcji.

Kolejną ważną częścią dysertacji jest przedstawienie specjalnie przygotowanego symulatora EMI w środowisku Matlab, do analizy układów cyfrowych. Pozwala on bardzo szczegółowo opisać parametry zarówno systemów synchronicznych jak i GALS, a następnie wygenerować wyniki poziomu szumów dla poszczególnych przedziałów częstotliwości. Umożliwia to analizę EMI w szerokim spektrum. Główną zaletą symulatora, szczególnie przydatną dla projektantów systemów cyfrowych, jest możliwość ustawienia przedziałów parametrów układu GALS, a następnie dzięki wykorzystaniu algorytmu hybrydowego taki ich dobór, aby EMI w danym układzie było jak najniższe.

W następnej części dysertacji szczegółowo opisane zostały układy GALS będące przedmiotem badań. Przedstawione zostały ich topologie, częstotliwości pracy zegarów, scenariusze transferu danych oraz charakterystyka poboru prądu przez poszczególne bloki. Część wykorzystanych układów GALS została opisane w języku VHDL, a następnie

ich zachowanie zasymulowano w programie Modelsim[2], w celu uzyskania rzeczywistych przebiegów pracy zegara.

W głównej, eksperymentalnej części pracy przedstawione zostały wyniki badań. W celu uzyskania bazy porównawczej zbadane zostały na początku układy synchroniczne. Następnie przeanalizowane zostały układy o strukturze GALS pod względem wpływu rozdrobnienia układu na redukcję EMI. Kolejnym krokiem było szczegółowe zweryfikowanie wpływu jittera (szybka fluktuacja fazy zegara taktującego) na redukcję interferencji elektromagnetycznej w układach GALS. Dodatkowo zebrane wyniki badań układów synchronicznych oraz GALS zostały ze sobą porównane, co pozwoliło na określenie możliwego stopnia redukcji EMI w układach GALS. Ten poziom redukcji wyniósł 26dB w stosunku do układu synchronicznego, który nie wykorzystuje żadnych technik redukowania EMI. Podane zostały także wyniki pracy algorytmu hybrydowego i poszczególne kroki realizacji algorytmu, w jaki sposób poszukiwane są korzystniejsze parametry pracy układu pod względem redukcji EMI w systemie cyfrowym. Przetestowane zostały także różne ustawienia algorytmu optymalizującego, szczególnie pod względem iteracji algorytmu wstępnego Monte Carlo.

Okazuje się, że dzięki zastosowaniu struktur GALS oraz faktu, w jaki sposób połączone są poszczególne moduły, wykorzystując naturę asynchronicznej pracy poszczególnych modułów uzyskać można znaczą redukcję EMI.

Podstawowe prace zostały wykonane w Instytucie Naukowo-Badawczym IHP im. Leibniz'a we Frankfurcie nad Odrą. Zostały tam, między innymi, przygotowane układy rzeczywiste bazujące na wynikach pracy, które potwierdzają poprawną pracę symulatora. Następnie prace kontynuowane były `w laboratoriach największej firmy telekomunikacyjnej na świecie NTT, mieszczącej się na obrzeżach Tokio w Japonii. Kolejne badania oraz budowa istoty algorytmu hybrydowego do optymalizacji EMI w układzie cyfrowym zostały przygotowane na Wydziale Informatyki Zachodniopomorskiego Uniwersytetu Technologicznego w Szczecinie.

Można łatwo dowieść, że wyniki prezentowanej pracy oznaczają, iż możliwe jest zmniejszenie mocy szczytowej głównego zasilania systemu liczącego poprzez zmianę jego struktury w strukturę GALS przy tej samej mocy obliczeniowej lub też możliwa sta-

[2] ModelSim - program do modelowania i debugowania układów cyfrowych, używany zwykle na etapie projektowania układów cyfrowych.

je się aplikacja systemu liczącego o większej mocy obliczeniowej przy zachowaniu już posiadanego (dotychczasowego) zasilania głównego. Zmniejszenie mocy zasilania lub możliwość zwiększenia mocy obliczeniowej przy niezmienionym zasilaniu głównym należy rozpatrywać równolegle ze zmniejszeniem prawdopodobieństwa wystąpienia błędów, jako praktyczne korzyści, bezpośrednio wynikające ze stosowania struktur GALS.

Jedynym innym znanym rozwiązaniem problemu zwiększania mocy obliczeniowej przy niezmienionym głównym zasilaniu są być dzisiaj jedynie komputery kwantowe, pracujące w okolicy zera bezwzględnego. Prace nad takimi komputerami prowadzone są w USA (MIT), ale znajdują się one dopiero na bardzo wstępnym etapie wdrożenia.

Acknowledgements

I would like to gratefully and sincerely thank PhD Eng. Leonard Rozenberg for his support, patience, understanding, and most importantly, his guidance during my PhD studies at West Pomerania University of Technology in Szczecin. I am truly convinced the he was the most suitable person to be my supervisor and oversee my progress. His mentorship was paramount in providing a well rounded experience consistent with my long-term career goals. He encouraged me to not only grow as a scientist and a lecturer, but also as a promising entrepreneur and an independent thinker. I doubt whether many graduate students are given the opportunity to develop their own individuality and self-sufficiency by being allowed to work with such independence. For everything you've done for me, Professor Rozenberg, I thank you.

I would also like to thank PhD Eng. Michal Twardochleb for his assistance and guidance in getting my graduate career started on the right foot and providing me with the knowledge regarding hybrid optimization. Additionally, I am very grateful for his support in writing articles and in publishing those.

Grateful acknowledgement is made to my Master thesis' supervisor at West Pomeranian University of Technology PhD, Eng. Piotr Dziurzański for giving me a chance to be a trainee in IHP (Institute for High Performance microelectronics, Frankfurt Oder) and being able to work on EMI in GALS systems, for support during that period and valuable comments on my work. I am sure that without his help I would not have come this far in my career. Having a chance to conduct my research abroad was a stepping stone to my future achievements. Thank you.

I would like to thank people who lightened and deepened my knowledge about GALS topic, enabled me to conduct initial studies regarding that systems in IHP (Institute for High Performance, Frankfurt Oder, Germany) and supported me during that period.

Great acknowledgements to Miloš Krstić for accepting me as a trainee in IHP at GALXY project, for helping me to start my career in that area and write papers for the PATMOS conference and Journal of Low Power Electronics and constant support during that time as my supervisor in IHP. He was my primary resource for getting my science

questions answered during that time. The given chance of working in IHP, allowed me to move further and continue my research and scientist career in Japan.

I would like to thank Eckhard Grass for his comments to my first papers regarding GLAS systems and also accepting me in IHP.

Finally, and most importantly, I would like to thank my fiancée Sylwia. Her support, encouragement, quiet patience and unwavering love were undeniably the great background to work on this dissertation. Her tolerance of my occasional absence at home is a testament in itself of her love and devotion. I thank my parents, especially my mum, for their faith in me and allowing me to be as ambitious as I wanted. It was under their watchful eye that I gained so much drive and an ability to tackle challenges head on.